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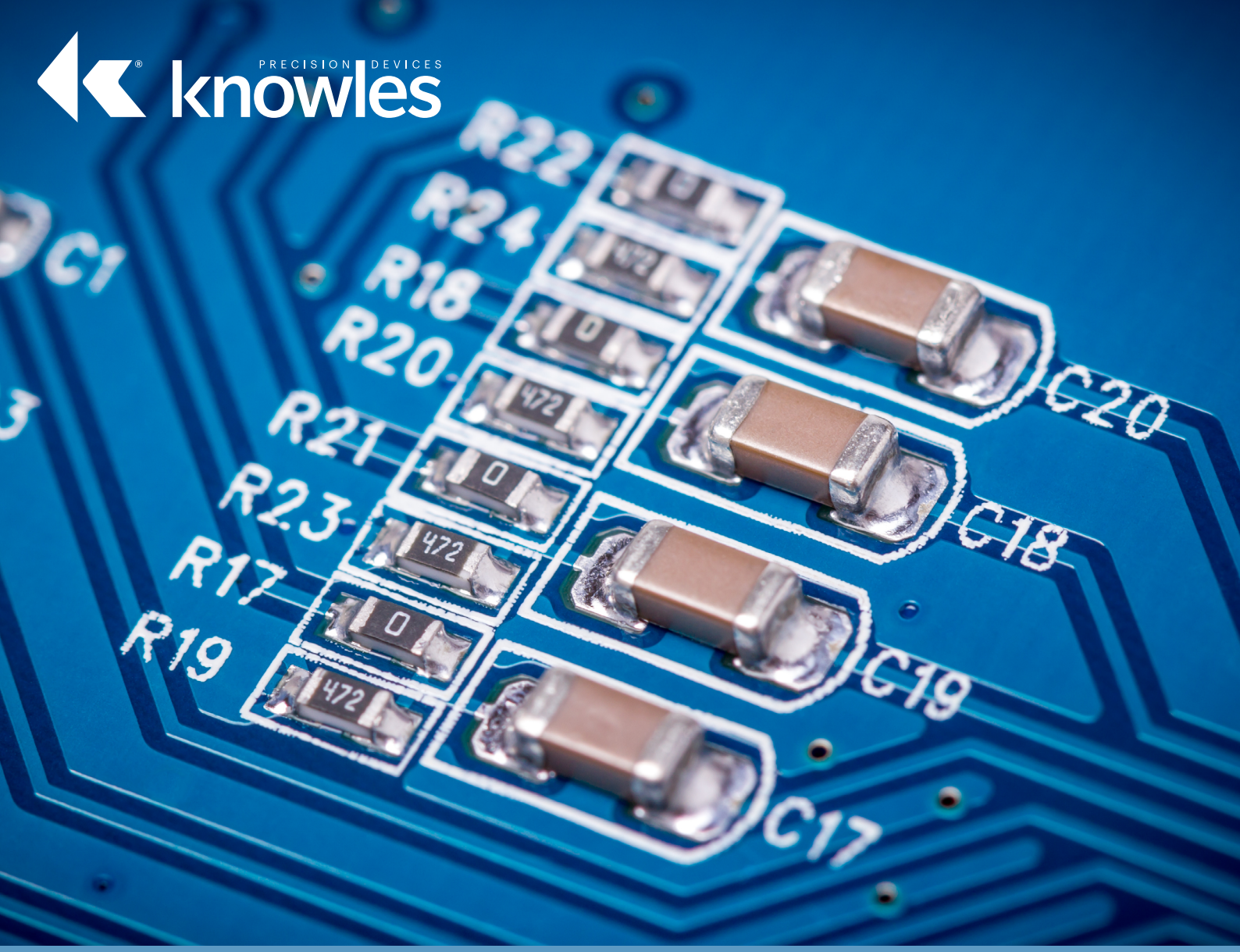

CAPACITOR FUNDAMENTALS EBOOK

A Comprehensive Guide to Selecting the Right Capacitor for Your Specific Application

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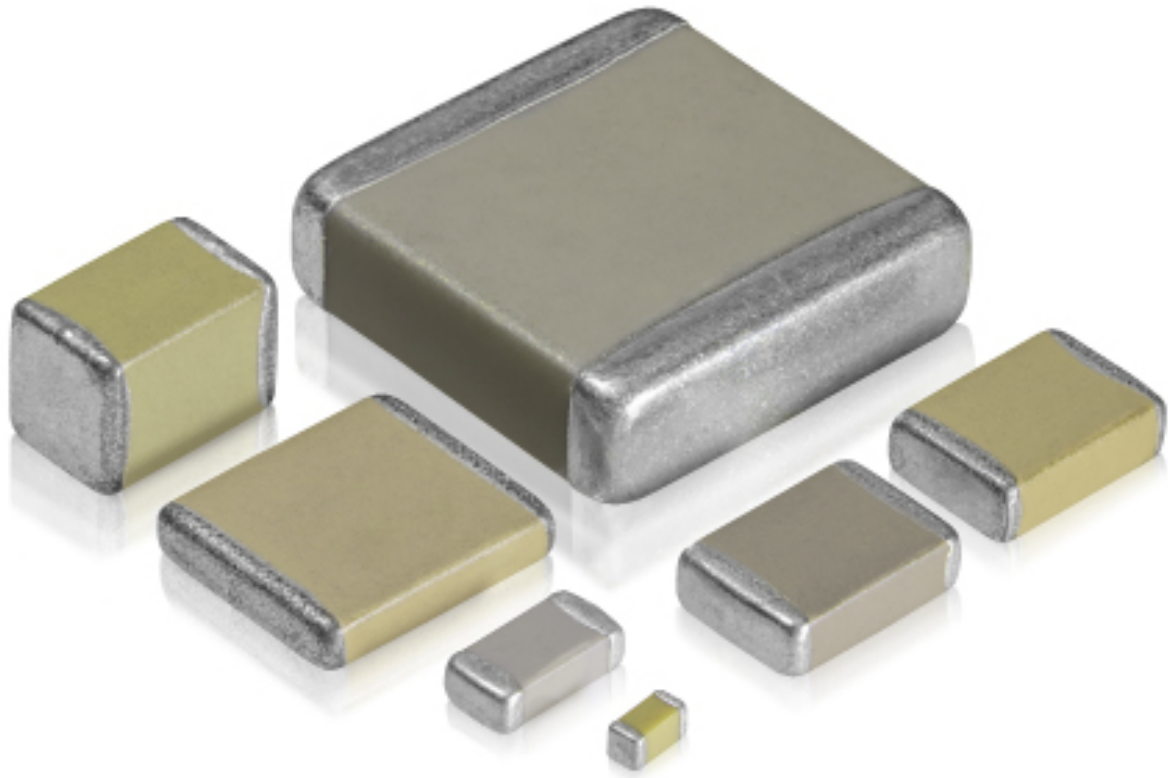
INTRODUCTION



At Knowles Precision Devices, our expertise in capacitor technology helps developers working on some of the world's most demanding applications across the medical device, military and aerospace, telecommunications, and automotive industries. Thus, we brought together our top engineers to compile their extensive knowledge into a comprehensive capacitor fundamentals eBook. This eBook will cover the ins and outs of capacitors, including their properties, product classifications, test standards, and use cases, with the goal of helping you make informed decisions when selecting your capacitor technology.

The Key Principles of Capacitance and How a Basic Capacitor Works

What is Capacitance?

Capacitance is the ability of a system (such as a component or circuit) to collect and hold energy in the form of electric charge. Capacitance value (C) is the ratio of the electric charge stored (Q) to the voltage applied (V), or C = Q/V. The charging current (I) is therefore expressed as I = dQ/dt = CdV/dt.

The value of capacitance is defined as one farad when the voltage across the capacitor is one volt, and a charging current of one ampere flows for one second.

C = Q/V = Coulomb/Volt = farad

Because the farad is a very large unit of measurement and is not encountered in practical applications, fractions of the farad are commonly used, such as:

- 1 picofarad (pF) = 10-12 farad
- 1 nanofarad (nF) = 10-9 farad
- 1 microfarad (μF) = 10-6 farad

> **Capacitance is the ability of a system to collect and hold energy in the form of electric charge.**

What is a Capacitor?

A capacitor is a passive electronic component that can store electric charge in an electric field. Unlike a battery, which stores energy and then gradually releases it, capacitors can be discharged in an instant. A basic unit consists of two conductors, or electrodes, separated from one another by an insulator, or dielectric (Figure 1).

Electrode Basics

To easily collect electric charge, the electrode must be a good conductor of electricity. Materials widely used in capacitor manufacturing include aluminum, copper, nickel, palladium, platinum, silver, and tantalum.

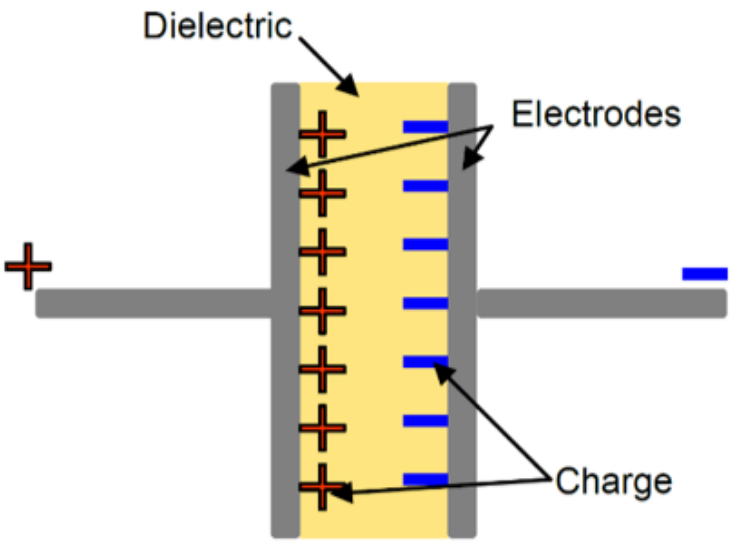


Figure 1: Selecting the Right Capacitor for Your Specific Application Needs

> **To easily collect electric charge, the electrode must be a good conductor of electricity.**

Depending on the manufacturing process used, the electrode may need to be unreactive with a high melting point. For example, the oxidizing atmosphere-fired ceramic capacitors manufactured at Knowles Precision Devices use a ceramic dielectric material with a sintering temperature of approximately 1,100 °C. To stop the electrode from melting during firing, a combination of silver and palladium is used. This method of manufacture is referred to as the precious metal electrode (PME) system.

Dielectric Basics

To store greater amounts of electric charge, the dielectric must be a good insulator, the properties of which largely determine the electrical behavior of the device. Dielectrics are characterized by their ability to store electrical charge and their intrinsic responses to an electric field, namely capacitance change, loss characteristics, insulation resistance, and dielectric strength, as well as the aging rate and the temperature dependence of these properties.

The dielectric constant, or relative permittivity ε_r, refers to a material's ability to store electrical energy in an electric field. It is the dominant characteristic that determines the capacitance value attainable at a given size and voltage. In other words, the higher the dielectric constant, the greater the capacitance for a particular capacitor design. Dielectric materials commonly used in capacitor manufacture include ceramics, porcelain, metal oxides, mica, and plastic film (Table 1).

DIELECTRIC CONSTANTS FOR VARIOUS MATERIALS	
Vacuum	1.0
Air	1.004
Mylar	3
Paper	4-6
Mica	4-8
Glass	3.7-19
Alumina (Al_2O_3)	9
Titania (TiO_2)	85-170, (varies with crystal axis)
Barium Titanate ($BaTiO_3$)	1500
Formulated Ceramics With Discrete Characteristics	20-18,000

Table 1: Dielectric Constants for Various Materials

For example, ceramic capacitors can be categorized into two main types based on if they're using C0G/NP0 dielectric (which have ε_r values between 20 and 100) or X7R dielectric (which have ε_r values of between 2,000 and 3,000).

> **To store greater amounts of electric charge, the dielectric must be a good insulator.**

Capacitor Construction

The most basic type of capacitor is a single layer that consists of a layer of dielectric material sandwiched between a positive and a negative electrode. A multilayer ceramic capacitor (MLCC) takes this concept and multiplies the number of layers to increase the available capacitance (Figure 2). Layers of ceramic are built up using a screen-printing process and are interleaved with electrodes of alternating polarity. The like polarity electrodes are then joined using a termination material. The termination can then be attached to wires or legs to form a radial leaded MLCC or electroplated to form a surface mount MLCC.

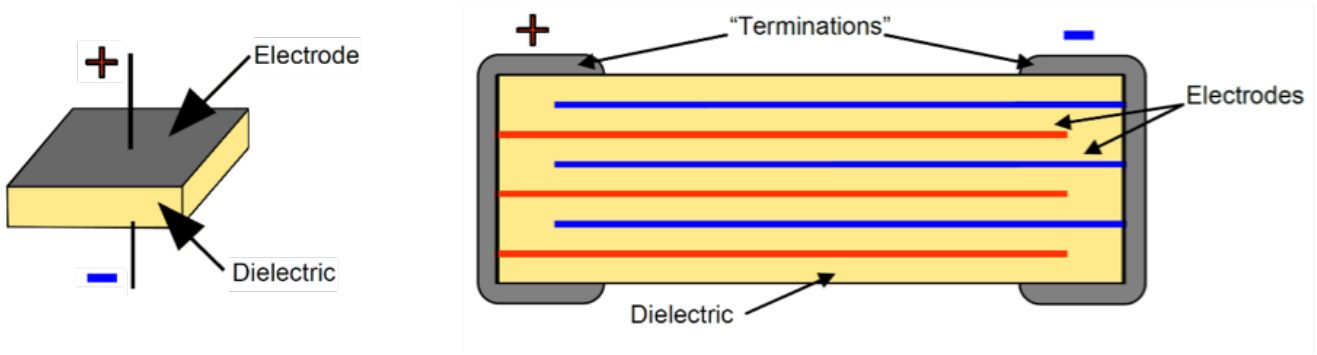


Figure 2. Single Layer Capacitor (Left) Versus a Multilayer Capacitor (Right)

How Capacitors Are Most Frequently Used in Electronic Circuits

Now that you have a basic understanding of capacitance and how capacitors work, let's focus on how capacitors are most frequently used in electronic circuits. As previously mentioned, capacitor technology covers a wide range of product types, based on a multitude of dielectric materials and physical configurations, yet all are basically storage devices for electric energy used in various applications in the electronic industry. The primary use cases for capacitors include:

- Discharge of stored energy
- Block of direct current (DC) signals
- Frequency discrimination
- Smoothing and energy storage

Let's take a closer look at each of these capacitor use cases.

Discharge of Stored Energy

Discharge or stored energy is one of the most basic applications of a capacitor. This involves the generation of a current pulse by discharge of a capacitor in the circuit. For example, in photography, the electronic flash on a camera must synchronize with the shutter opening to emit a burst of light in a fraction of a second. A large capacitor is charged to several hundred volts using the camera's battery, and when the shutter button is pressed, the energy is instantly discharged through the xenon flash tube to produce a bright flash. After the shot is taken, the capacitor must spend some time recharging before it can be used again (Figure 3).

Figure 3: Photography is a Common Consumer Application Where Capacitors are Used

Blocking of DC Signals

Another important use of capacitors is to stop DC but allow alternating current (AC) from one part of an electronic circuit to another. Capacitors, once charged, act as high impedance elements and thereby block the DC from specified portions of a circuit.

Figure 4: Another Common Consumer Application Where Capacitors are Used

In an AC circuit with varying (alternating positive and negative) voltage applied, a current will flow first in one direction, then in the other as the capacitor charges and discharges. This allows alternating current to appear on either side of the component so that sections of a circuit can be coupled together. The current does not flow physically through the capacitor since the dielectric is an insulator. Continuous current surges are the result of the change in voltage across the capacitor.

By blocking the DC and permitting the passage of AC, the device can be used inparallel with another circuit element to allow AC to bypass the element without passing the DC portion of the signal. Capacitors are regularly used this way in television, radio, and audio amplifiers (Figure 4).

> **Capacitors, once charged, act as high impedance elements and thereby block the DC from specified portions of a circuit.**

Frequency Discrimination

Because of its capacitance value, a capacitor is nonresponsive to low frequency signals, making it useful for segregating an input signal with mixed frequencies. For capacitors in an AC circuit, the current flow increases with frequency, whereas the capacitance reactance (or the resistance to flow of AC) is inversely proportional to the capacitance value. Therefore, a capacitor can be designed to have minor opposition to current flow for the high frequency portion of the signal while offering greater opposition to the lower frequency current, thus making it useful for filtering out a desired frequency range.

Such capacitors are commonly used to detect radio frequency as part of the tuning circuit for television and radio devices. They can also filter out frequencies that may interfere with the equipment's functionality.

Smoothing and Energy Storage

Capacitors are often used to stabilize the voltage to sensitive devices by absorbing excess energy generated from undesired transient voltage surges and eliminating arcing of contact points. This particular application accounts for a large portion of all MLCCs used (Figure 5). For example, a smoothing capacitor may be used close to computer memory chips to ensure that the chip operating voltage stays constant, in spite of the electrical activity going on all around. The same property is also used to smooth the outputs from power supplies and voltage converters.

Figure 5: MLCCs Used for Smoothing and Energy Storage

Factors Affecting Capacitance

As with any electronic device component, there will always be external factors and device limitations to take into consideration when deciding which type of capacitor is right for your application. Let's start by diving into the background for how capacitance is calculated for any capacitor. For any given voltage, the capacitance value of the single-plate device (Figure 6) can be calculated from the geometry and dielectric constant of the device as follows:

$$C = KA/f(t)$$

where

C = capacitance
K = dielectric constant
A = area of electrode
t = thickness of dielectric
f = conversion factor

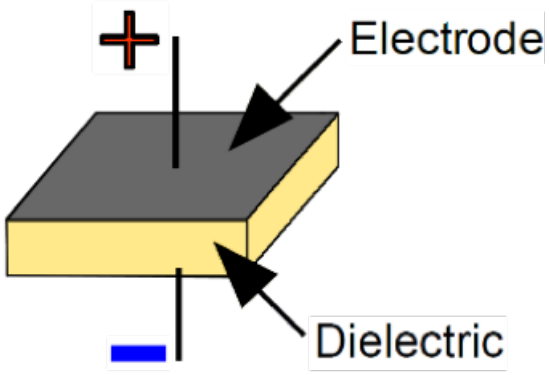


Figure 6: A Diagram of a Single-Layer Capacitor

In the English system of units, f = 4.452, the dimensions for A and t are listed in inches, and the capacitance value is expressed in picofarads (pF). Therefore, for a device such as the example shown in Figure 6 with a 1.0" X 1.0" area, 0.056" dielectric thickness, and a dielectric constant of 2500, the capacitance comes out to:

$$C = 2{,}500\ (1.0)(1.0)/4.452\ (0.056) = 10{,}027\ pF$$

Utilizing the metric system, the conversion factor is f = 11.31 and dimensions are used in centimeters. The capacitance comes out to the same value of:

$$C = 2{,}500\ (2.54)(2.54)/11.31\ (0.1422) = 10{,}028\ pF$$

As seen in the above equation, greater capacitance can be achieved by increasing the electrode area while decreasing the dielectric thickness. Since increasing the area in a single plate device with thinner dielectric will produce a fragile, unusable component, the concept of stacking capacitors in a parallel array was conceived to produce a physically sound device with more capacitance per unit volume, as illustrated in Figure 7.

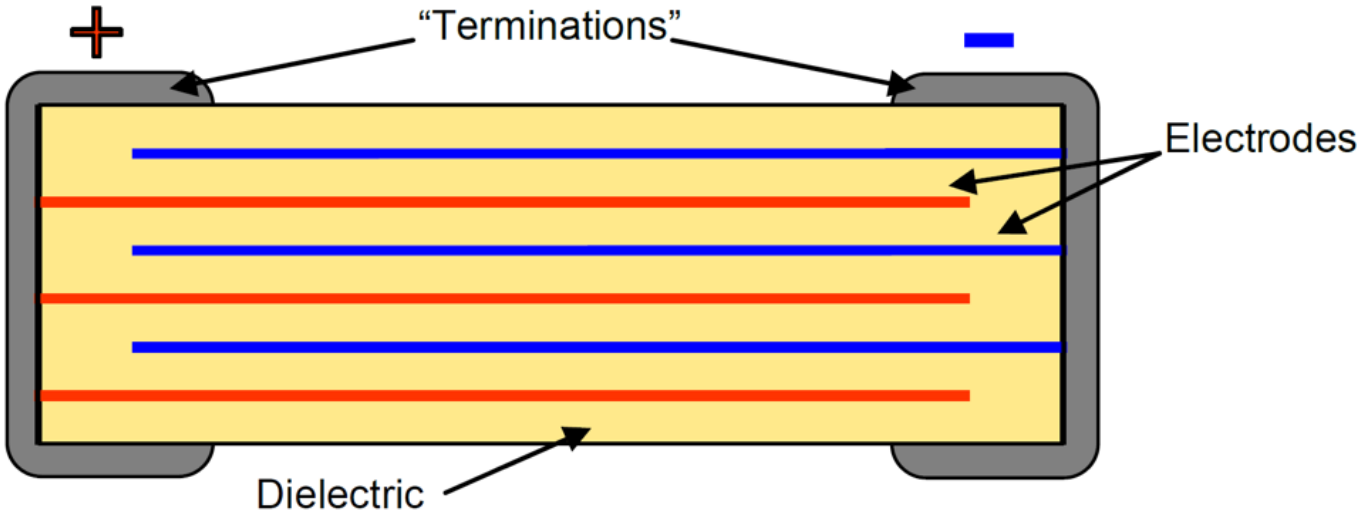


Figure 7: A Diagram of an MLCC

In this multilayer configuration, the area A is increased by virtue of many electrodes in parallel arrangement, using a construction that permits a very thin dielectric thickness between opposing electrodes. Therefore, the capacitance C is enlarged by the factor N (number of dielectric layers) and reduced dielectric thickness t', where A' is now the area of overlap of opposing electrodes:

$$C = KA'N/4.452(t')$$

The capacitance value previously obtained for the 1.0" x 1.0" x 0.056" single plate device can now be produced with the same dielectric in a multilayer unit of only 0.050" x 0.050" x 0.040" dimensions and 30 dielectric layers of thickness 0.001" (where the electrode overlap A' is 0.030" x 0.020").

$$C = 2{,}500\ (0.030)\ (0.020)\ 30/4.452\ (0.001) = 10{,}107\ pf$$

This example shows how multilayer construction can deliver the same capacitance in a volume 700 times smaller than that of the single plate device. Chip capacitors are therefore designed and manufactured to maximize the volumetric efficiency of capacitance by optimizing the geometry and by selecting dielectric formulations with a high dielectric constant and general electrical properties (e.g., good insulation resistance and dielectric strength), which permit very thin layer construction.

> **Higher voltage capacitors need greater dielectric thickness, which has the effect of reducing the capacitance in a nonlinear fashion.**

As a final consideration, these relationships have knock-on effects on the amount of capacitance available at set sizes and voltages. Smaller footprint and restricted thickness limit the available capacitance value. Higher voltage capacitors need greater dielectric thickness, which has the effect of reducing the capacitance in a nonlinear fashion.

For example, increasing the voltage from 1,000 V to 2,000 V requires a typical doubling of dielectric thickness; this, in turn, means that only half the number of electrodes can fit into a set thickness. Since capacitance is directly proportional to overlap area and inversely proportional to dielectric thickness, the overall capacitance available in a given size at 2,000 V is now roughly 25 percent of that at 1,000 V.

In the next section we expand beyond the factors effecting capacitance with an in-depth look at how a variety of factors can affect the behavior of a material when an external electric field is applied on it, which is also known as dielectric polarization.

Defining Dielectric Polarization

When an electric field is applied to a capacitor, the dielectric material (or electric insulator) becomes polarized, meaning the negative charges in the material orient toward the positive electrode and the positive charges shift toward the negative electrode. Since charges are not free to move in an insulator, the polarization effect that opposes the applied field draws charges onto the electrodes, thus storing energy in the capacitor.

The more easily a material can be polarized, the greater the amount of charge that can be stored in the capacitor. This ability to store energy in an electric field is referred to as the dielectric constant K, or relative permittivity ε_r. The degree of polarization P is related to the dielectric constant K and the electric field strength E as follows:

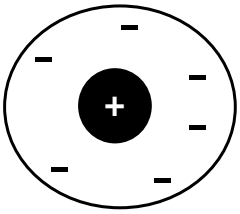
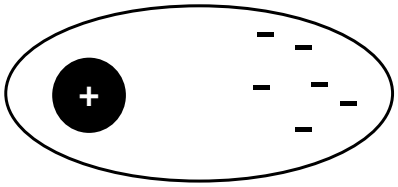
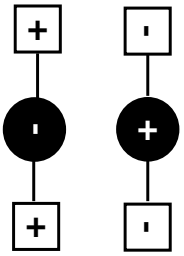
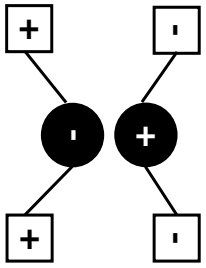
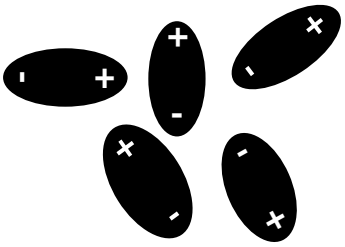
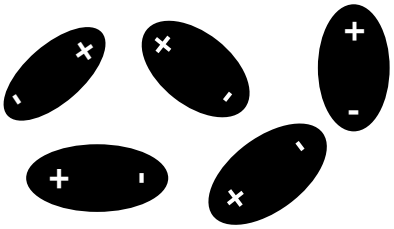
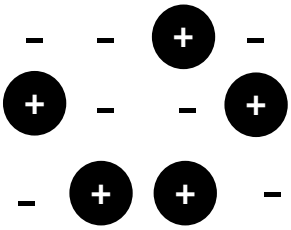
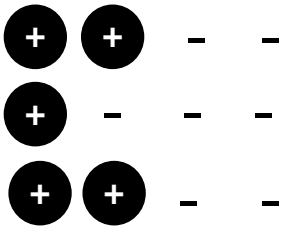
$P = \varepsilon_0 (K-1) E$
where ε_0 is a physical constant known as the vacuum permittivity

> **The more easily a material can be polarized, the greater the amount of charge that can be stored in the capacitor.**

The total polarization of a dielectric comes from the sum of the following four sources of charge displacement (Figure 8):

- Electronic displacement Pe —This effect occurs in all atoms under the application of an electric field. The nucleus of the atom and the center of its electron cloud shift away from each other, creating a tiny dipole with very small polarization effect.
- Ionic displacement Pi—In ionic solids, such as ceramic materials, the ions are symmetrically arranged in a crystal lattice with a net zero polarization. Once an electric field is applied, the cations and anions are attracted to opposite directions. This creates a relatively large ionic displacement (compared to electronic displacement), which can give rise to high dielectric constants in ceramics popularly used in capacitors.
- Orientation of permanent dipoles Pd—Certain solids have permanent molecular dipoles that, under an electric field, rotate themselves in the direction of the applied field, creating a net average dipole moment per molecule. Dipole orientation is more common in polymers since their atomic structure permits reorientation.
- Space charge displacement Ps—In ceramics, this phenomenon arises from extraneous charges that come from contaminants or irregular geometry in the interfaces of the polycrystalline solids. These charges are partly mobile and migrate under an applied field, causing this extrinsic type of polarization.

$Pt = Pe + Pi + Pd + Ps$

Polarization Mechanisms		
	No E field ($E = 0$)	Local E field ($E \neq 0$)
Electronic		
Atomic or Ionic		
Orientation or Dipolar		
Interfacial		

How Does Frequency Affect Polarization and Dielectric Loss?

Interestingly, each type of polarization has a different time response capability to an applied field frequency, which means the net effective of polarization to the dielectric constant is frequency dependent. More specifically:

- Electronic displacement is very rapid, so this polarization occurs at frequencies of up to 1017 Hz.
- Ionic polarization is a bit slower and occurs at frequencies up to 1013 Hz.
- Dipole polarization occurs at frequencies less than 1010 Hz.
- Space charge polarization is the slowest and occurs at less than 104 Hz.

> **The dielectric constant, and therefore the capacitance value, always decreases with increased frequency.**

Thus, the dielectric constant, and therefore the capacitance value, always decreases with increased frequency, since the polarization mechanisms become less effective (Figure 9).

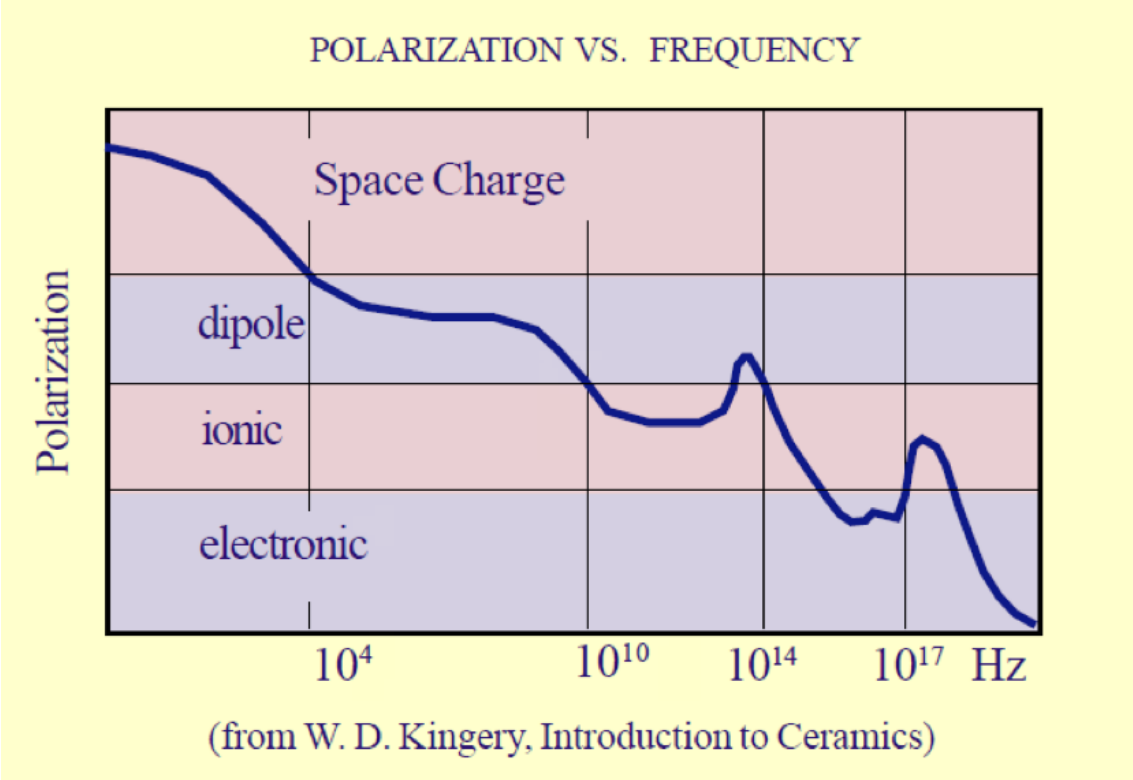


Figure 9: The Effect of Frequency on Polarization Mechanisms

> **Real-world dielectrics are not perfect, and therefore the lag or 'relaxation time' of the polarization mechanisms with frequency generates dielectric losses.**

In an AC circuit, the voltage and current across an ideal capacitor are 90 degrees out of phase. However, real-world dielectrics are not perfect, and therefore the lag or "relaxation time" of the polarization mechanisms with frequency generates dielectric losses. The angle by which the capacitor's current is out of phase from the ideal can be determined, and the tangent of this angle is a material property called the loss tangent (Tan δ) or dissipation factor. In practice, materials with higher dielectric constants (and therefore high polarization mechanisms) display higher dissipation factors (Figure 10).

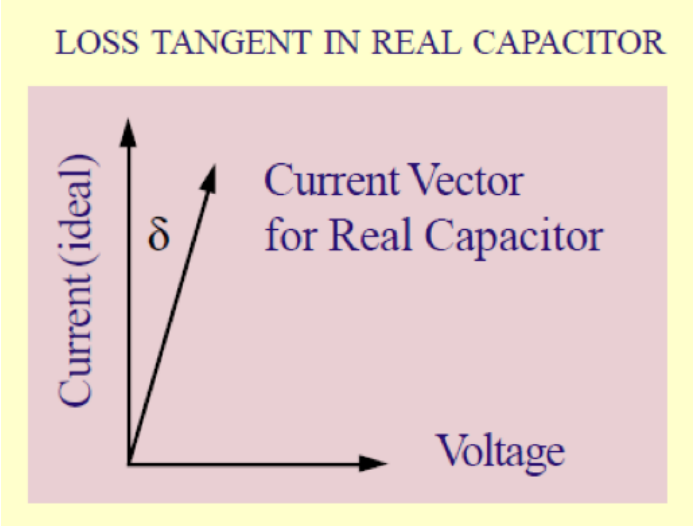


Figure 10: Tangent Loss or Dissipation Factor of a Real-World Capacitor

The frequency at which a dielectric is used has an important effect on the polarization mechanisms, notably the relaxation time displayed by the material when following field reversals in an alternating circuit. The following are three possible scenarios that can occur as a result of varying relaxation times:

- Case 1: If the relaxation time for polarization is much longer and slower than the field reversals, the ions cannot follow the field at all and losses are small.
- Case 2: If the relaxation time is much faster than the field reversals, the polarizing processes can easily follow the field frequency and losses are small.
- Case 3: If the relaxation time and field frequency are the same, the ions can follow the field but are limited by their lag, thus generating the highest loss with frequency.

> **Dielectric losses are highest at the frequency where the applied field has the same period as the relaxation process.**

Therefore, dielectric losses are highest at the frequency where the applied field has the same period as the relaxation process. Ceramic dielectric formulations always show a range of relaxation times over the frequency spectrum, since these materials consist of polycrystalline matter. In high-frequency applications, this parameter is often known as the Q factor, which is the reciprocal of the loss tangent: $Q = 1 / (\tan \delta)$.

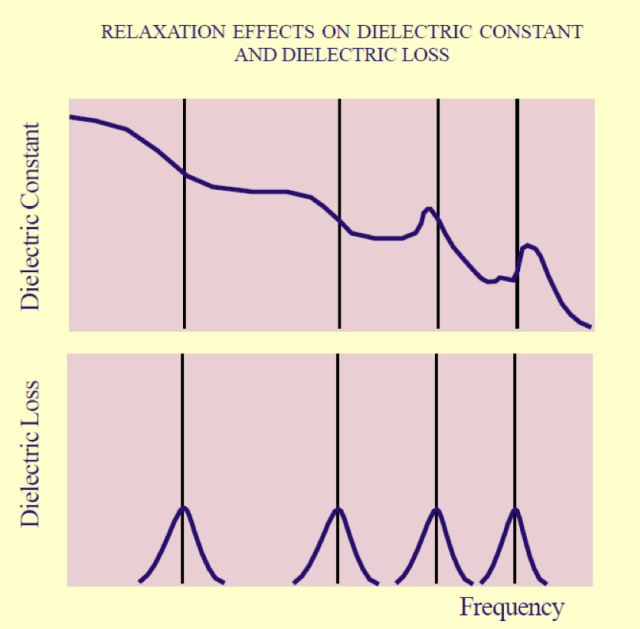


Figure 11: Changes in Dielectric Constant and Dielectric Loss Caused by Frequency

Now that we've covered the basics of dielectric polarization and the relationship with frequency, let's examine the following five dielectric properties that affect capacitor performance:

- Insulation resistance
- Dielectric strength
- Capacitor aging
- Electromechanical coupling
- Dielectric absorption

Dielectric Properties

Insulation Resistance

The perfect insulator has no movement of free electrons and possess infinite electrical resistivity. However, real-world insulators contain impurities and defects in their atomic lattice structure that give rise to charge carriers, resulting in some amount of leakage current under an applied electric field. Insulation resistance (also known as the parallel or shunt resistance of a capacitor) is a measure of the capability of a material to withstand leakage of current and is not the same as the series resistance of a capacitor. The insulation resistance of chip capacitors is dependent on the dielectric formulation, processing, and temperature at measurement (since resistivity decreases with temperature).

Using Ohm's Law, which is a formula used to calculate the relationship between voltage, current and resistance in an electrical circuit, and the relationship of capacitance to geometry, we can demonstrate that capacitance and leakage current are directly proportional to one another. Since leakage current and insulation resistance are inversely proportional, it stands to follow that the capacitance of a capacitor is also inversely proportional to insulation resistance. Therefore, Electronic Industries Alliance (EIA) specifications establish minimum standards for insulation resistance (IR) as the product of the resistance (R) and capacitance (C), or RxC (Table 2).

Capacitance	Min IR (GΩ)	Min RxC (ΩF) @ 25°C
0.1 pF to .010µF	100.00	1000
.015	66.67	
.022	45.45	
.033	30.30	
.047	21.28	
.068	14.71	
.100	10.00	
.150	6.67	
.220	4.55	
.330	3.03	
.470	2.13	
.680	1.47	
1.00	1.00	
etc.	etc.	

Table 2: Minimum Insulation Resistance Standards vs Capacitance

> **Real-world insulators contain impurities and defects in their atomic lattice structure that give rise to charge carriers, resulting in some amount of leakage current under an applied electric field.**

In addition to material and geometric variables, insulation resistance is also affected by the following:

- Different resistivity at the dielectric's surface due to absorbed impurities or water moisture
- Physical defects in the dielectric formulation, which are proportional to the chip volume and complexity of its structure

Therefore, larger units with a larger electrode plate area and more electrode layers may possess a lower resistivity, and thus lower insulation resistance than predicted for smaller devices.

Dielectric Strength

The dielectric strength is a measure of the material's ability to withstand a large field strength without electrical breakdown, usually expressed in volts per mil (1/1000 of an inch) or volts per cm of dielectric. Dielectric failure occurs in insulators when the applied field reaches a threshold where the restoring forces within the crystal lattice are overcome and an avalanche of free electrons is generated, resulting in a high burst of current that punctures the dielectric. In addition, high voltage stress creates heat and lowers the resistivity of the material, which may lead to a leakage path at the weakest portion of the dielectric.

The dielectric strength is diminished by physical defects in the microstructure of the material, and therefore the thicker the dielectric, the greater the probability of random defects and the lower the dielectric strength. Similarly, dielectric strength is inversely proportional to the electrode layer count of a chip capacitor and to its physical size (Figure 12).

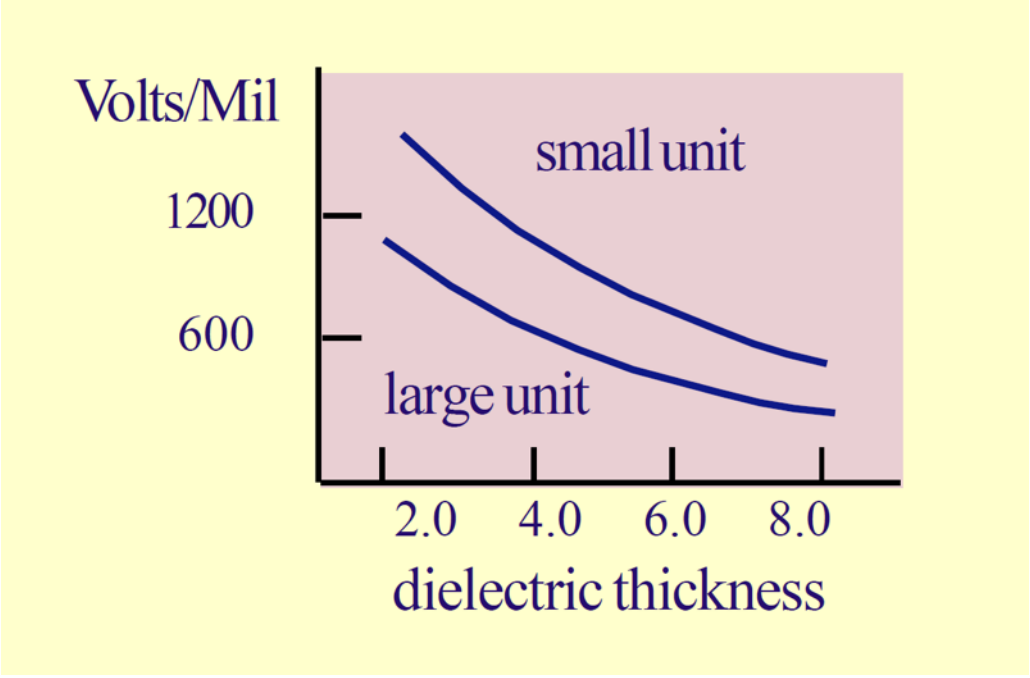


Figure 12: Dielectric Strength vs Dielectric Thickness

Chip capacitors are designed with a margin of safety based on the above considerations to preclude failure in use and at the dielectric withstanding voltage test, which typically is 2.5 times the working voltage of the device.

Capacitor Aging

Ceramic capacitors made with ferroelectric formulations exhibit aging – which involves changes to the dielectric's crystal structure caused by temperature and time. Ferroelectric materials exhibit spontaneous polarization, where dipoles naturally form without an applied electric field. However, over time the ions in the crystal lattice shift and stabilize to positions of lower potential energy. This degradation of the domains of polarization causes a logarithmic aging of the dielectric constant, such that the majority of capacitance loss occurs in the first 10 hours of age.

Aging in ferroelectric dielectrics can be reversed by bringing the material to a greater temperature than its Curie point (e.g. approximately 120°F for barium titanate [BaTiO3]) and then cooling it back down. This phenomenon can be observed shortly after soldering the capacitor, causing the dielectric to reform the domains of spontaneous polarization, recover its capacitance value, and recommence the aging process. Capacitor manufacturers compensate for capacitance loss of ferroelectric dielectrics by adjusting the testing limits, such that units do not age out of tolerance over a long time period.

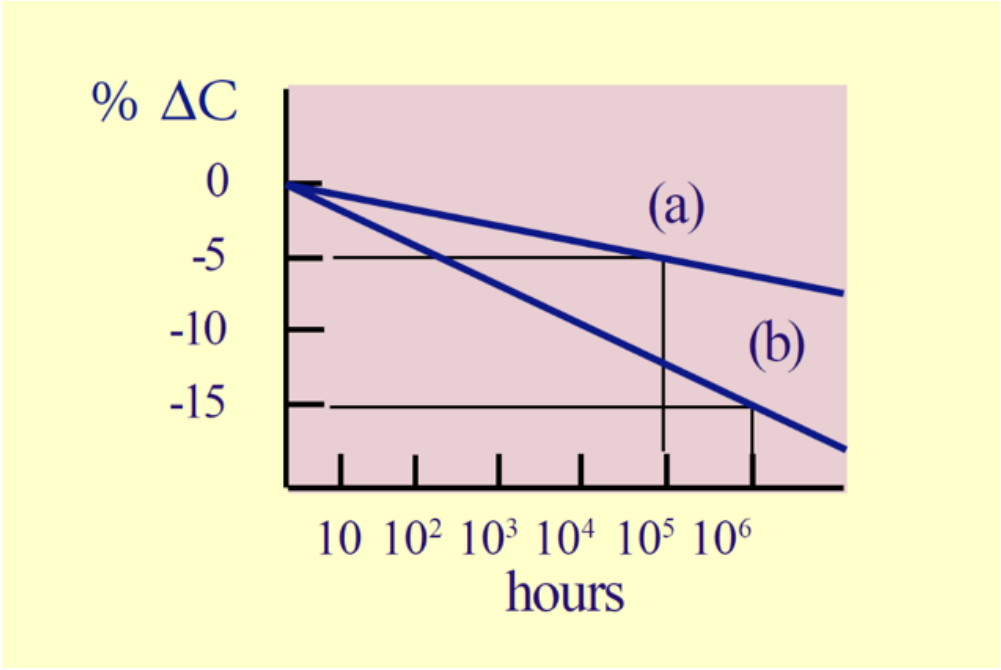


Figure 13: Ferroelectric Aging Shown as Percent Change in Capacitance (%ΔC) Over Time

> **Ceramic capacitors made with ferroelectric formulations exhibit aging – which involves changes to the dielectric's crystal structure caused by temperature and time.**

Electromechanical Coupling

All dielectric materials display mechanical deformation or a change in shape when under the influence of an electric field. This behavior, known as electrostriction, is caused by ionic polarization, where the cations and anions within the crystal lattice are attracted to opposite directions, in crystals that have a center of symmetry. Electrostriction is a one-sided relationship because an electric field causes physical deformation, but applying mechanical stress does not induce an electric field since the charged centers are not displaced.

On the other hand, piezoelectric materials display a two-sided relationship between mechanical stress and polarization. Because the crystals lack a center of symmetry, the centers of charge shift if the material is compressed, thus producing a dipole moment that results in polarization. This effect is a true linear coupling, as the elastic strain observed is directly proportional to the applied field intensity, and the polarization obtained is directly proportional to the applied mechanical stress (Figure 14).

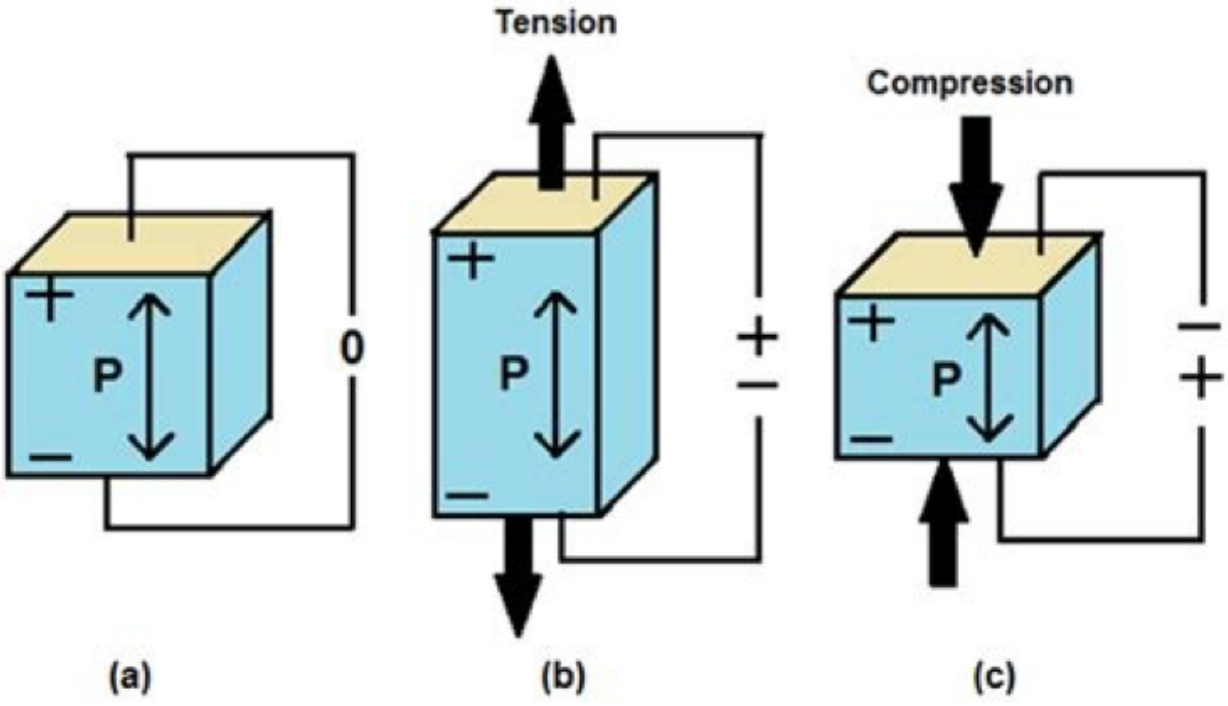


Figure 14: Different Piezoelectric Responses to Applied Mechanical Stress (source: ResearchGate)

Dielectric Absorption

Dielectric absorption is the measurement of a residual charge on a capacitor after discharge, expressed as the percent ratio of the residual voltage to the initial charge voltage. This residual voltage is caused by the relaxation phenomena of polarization, which was covered previously in this eBook. Just as the polarization mechanisms can lag the applied field, the inverse situation also applies, where depolarization or discharge can also lag. In fact, a small fraction of the polarization may persist long after discharge, which can be measured on the device with a high impedance voltmeter. Dielectrics with higher dielectric constants, and therefore more polarizing mechanisms, typically display more dielectric absorption than materials with lower dielectric constants.

Let's look at how these dielectric properties differ between ferroelectric ceramics and liner dielectrics.

Characteristics of Ferroelectric Ceramics

Paraelectric dielectrics have a linear relationship between polarization and an applied electric field, such that an applied field causes displacement in the ions (i.e. ionic polarization) and then the removal of the field causes the ions to return to their original positions. However, ferroelectric dielectrics such as BaTiO3 exhibit spontaneous polarization caused by permanent dipoles that exist without an applied field. Therefore, ferroelectric ceramics display a nonlinear hysteresis effect of polarization with an applied field (Figure 15).

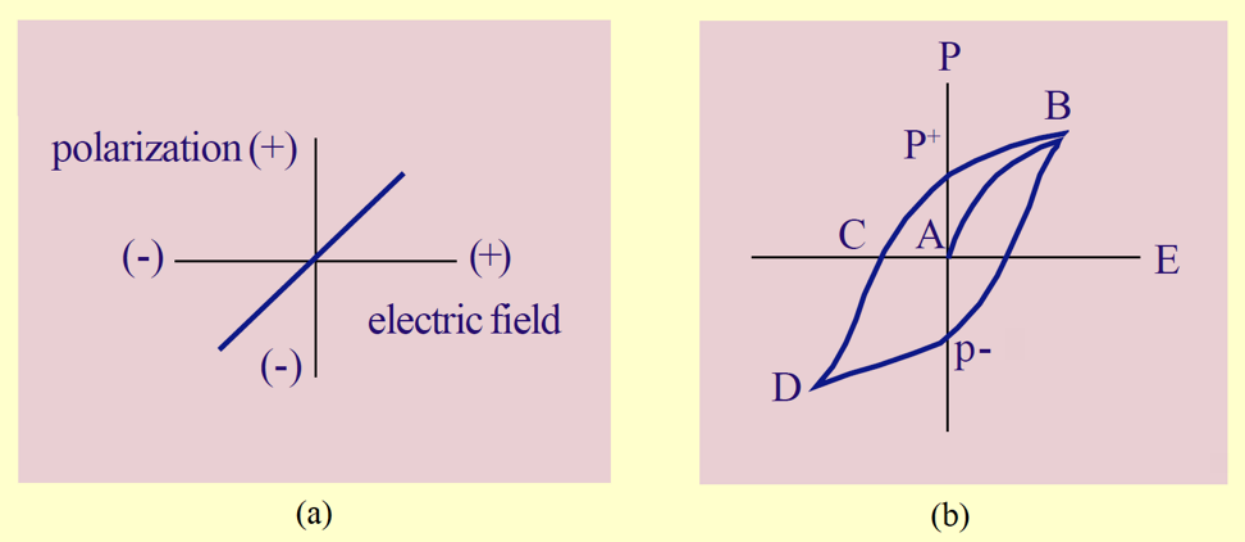


Figure 15. Polarization of Linear Dielectric (a) vs. Ferroelectric Dielectric (b)

Hysteresis Loop in Ferroelectrics

Let's look at a step-by-step breakdown of the ferroelectric hysteresis loop with regards to polarization versus an applied electric field as seen in Figure 15b:

1. Point A: Upon creation, the ferroelectric domains, or areas of oriented spontaneous polarization, are randomly oriented and the material has no polarization.
2. Point B: If an external field is applied, the Ti atoms in BaTiO3 become displaced in the direction of the field, creating a rapid and major polarizing effect until maximum orientation with the field is achieved.
3. Point C: Removing the field will eliminate any normal ionic polarization, but the Ti atoms remain in their newly oriented state, resulting in a remnant polarization P+. To remove this polarization, an opposing field (point C) must be applied to revert half the volume of the domains towards the new field direction.
4. Point D: Continuation of the field cycle inverts the polarization to its maximum, and the removal of the negative field leaves a net polarization P-.

Further cycles of the electric field retrace the original path, creating a continuous hysteresis effect. In order to reach zero polarization at 0 volts (point A) again, the dielectric must be heated past its Curie temperature to generate a new system of random ferroelectric domains.

The Effect of Temperature on Ferroelectric Hysteresis Loops

The hysteresis loop will vary in shape with temperature. At lower temperatures, there is less thermal motion of atoms, so a greater electric field is required to orient the domains. At high temperatures, the applied field required for polarization decreases until it becomes nearly linear at the Curie point (Figure 16).

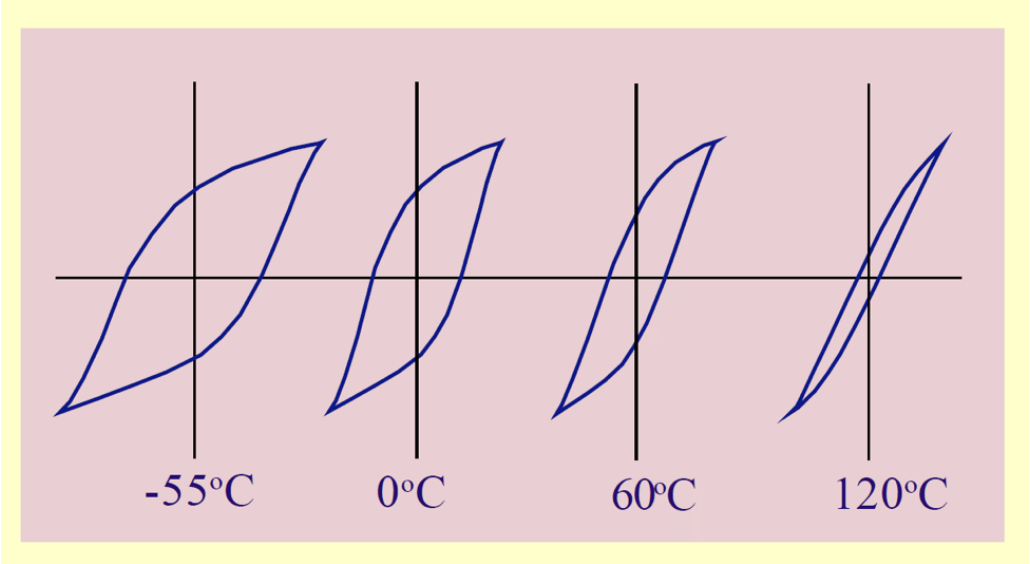


Figure 16: Hysteresis Loop at Various Temperatures

This change is caused by the different phase transformations that BaTiO3 goes through at different temperatures, as seen in Figure 16. At the 120°C Curie point, the material transforms from a non-polar cubic to a polarized tetragonal structure. Upon further cooling, a change from tetragonal to orthorhombic occurs at 0°C, which then transforms to the rhombohedral crystal habit at -90°C (Figure 17).

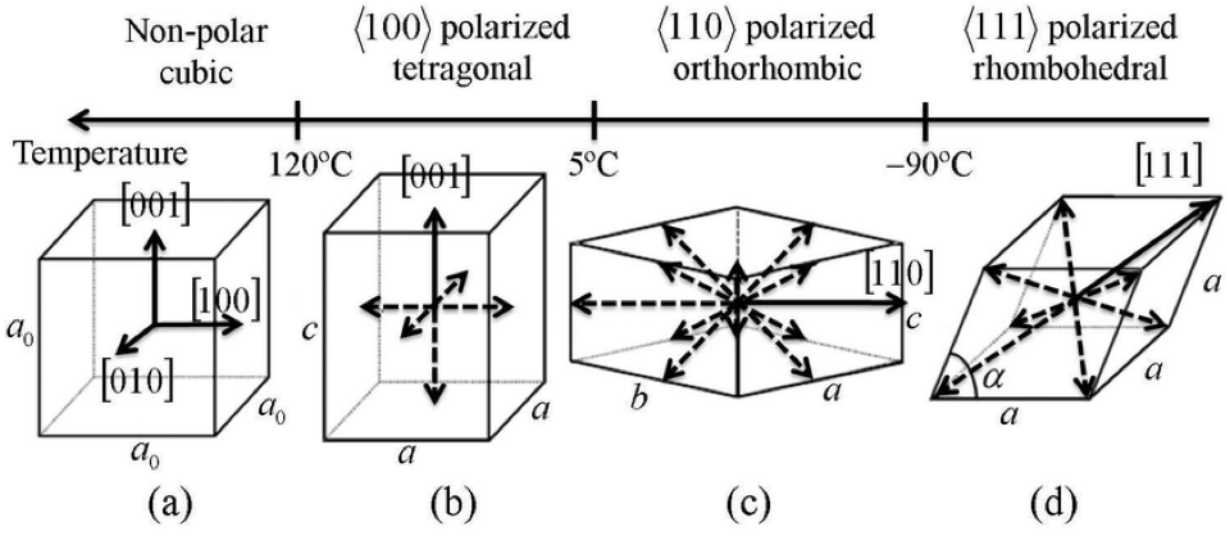


Figure 17. Phase Transformations of BaTiO3 (source: University of Oxford)

These phase changes with temperature variation are accompanied by changes in the dielectric constant K of the ceramic. Variations in the electrical properties of $BaTiO_3$ present some obvious challenges. Polarization, and therefore the dielectric constant, is a function of the electric field intensity. Plus, the dielectric constant is highly temperature dependent, and practical applications specify stability over a -55°C to 125°C temperature range. Finally, ferroelectric ceramics display aging and piezoelectric effects.

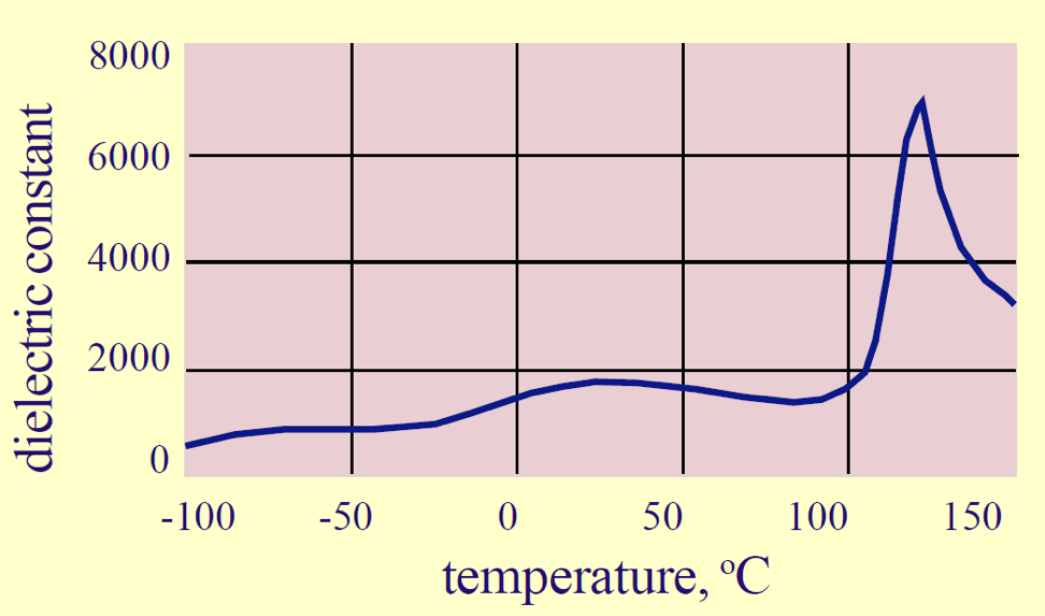


Figure 18. Changes in $BaTiO_3$ Dielectric Constant With Varying Temperature

Using Additives for Greater Stability

Fortunately, other elements can be incorporated into the $BaTiO_3$ crystal structure to modify its properties. Lots of research has gone into optimizing these materials with the hopes of altering the dielectric behavior and temperature dependence of $BaTiO_3$.

"Shifter" additives such as strontium titanate ($SrTiO_3$) and calcium ziconate ($CaZrO_3$) are used to shift the Curie point such that the high K properties of the ferroelectric work at or near room temperature, whereas lead titanate ($PbTiO_3$) is used to transfer the Curie point to higher temperatures. "Depressors" such as magnesium ziconate ($MgZrO_3$) and bismuth tin oxide ($Bi_2Sn_3O_9$) depress the dielectric constant peak at the Curie point to provide a more stable K value over temperature. Other additives affect the microstructure by isolating or reducing the ferroelectric grains, thus decreasing the dielectric constant, aging rate, and piezoelectric effects. Much effort has gone into optimizing these materials and using them in careful proportions to maximize the usefulness of the dielectric for practical applications.

Fortunately, other elements can be incorporated into the $BaTiO_3$ crystal structure to modify its properties.

Characteristics of Linear Dielectrics

Non-ferroelectric dielectrics show a linear relationship of polarization to voltage (as seen in Figure 15) and are formulated to have a linear temperature coefficient. These materials consist primarily of titanium dioxide (TiO_2) and therefore exhibit lower dielectric constant (less than 150). More importantly, they have lower dielectric loss and no aging of capacitance with time. These properties, along with negligible dependence of capacitance with voltage or frequency, make these dielectrics useful in capacitor applications where close tolerance and stability are required.

Linear dielectrics are also referred to as temperature compensating capacitors since the temperature coefficient can be modified to give predictable slopes of the temperature coefficient of capacitance (TCC) over the standard -55°C to 125°C range. These slopes vary from approximately a positive of 100 parts per million per degree Celsius (ppm/ °C) to a slope of typically negative 750 ppm/ °C. These values are reported as P100 or N750 respectively. A flat slope, which is neither positive nor negative, is a negative-positive-zero (NPO or COG) and is one of the most common of all dielectric characteristics (Figure 19).

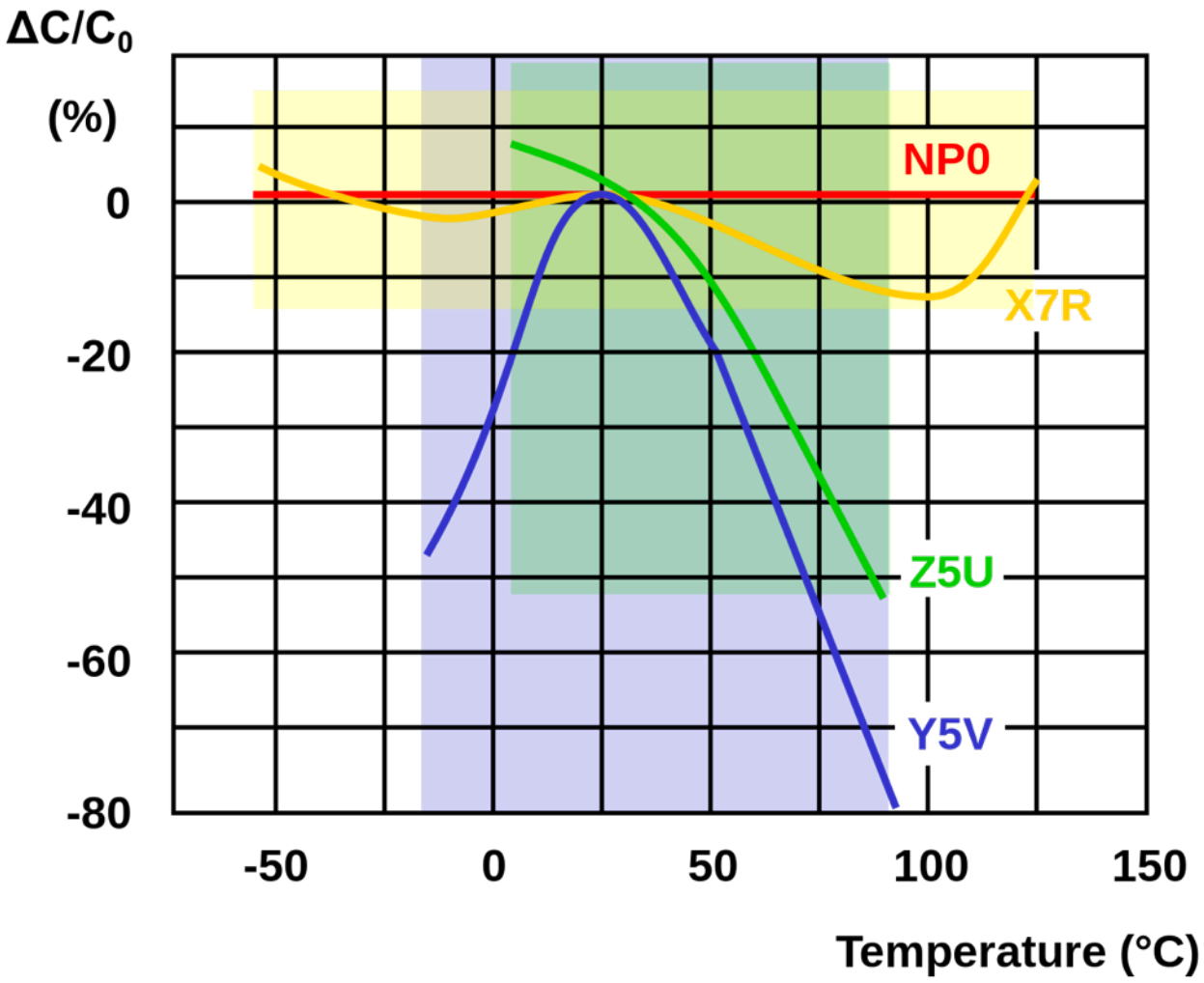


Figure 19. Capacitance Varying with Temperature for Different Capacitor Types (source: Wikipedia)

A series of linear dielectrics known as the extended TCC type range from N750 to as negative as N5600. These values are obtained by using dielectrics with the Curie point well below the -55°C lower limit of the MIL specifications, such that the TCC portion between -55°C to 125°C is approximately linear.

Now that you have a good understanding of both ferroelectrics and linear dielectrics, let's discuss the different types, or classes, of dielectrics.

> **There is a trade-off where dielectrics with a higher dielectric constant K have greater losses and less stability in terms of temperature, voltage, and time.**

Dielectric Classes Overview

Different dielectric materials all have their own characteristics and practical uses. Generally speaking, there is a trade-off where dielectrics with a higher dielectric constant K have greater losses and less stability in terms of temperature, voltage, and time. Dielectric formulations are classified in the industry by their temperature coefficient of capacitance (TCC), or how much capacitance changes with temperature. Class I and II are commonly used for making ceramic chip capacitors, while Class III is used for making disc capacitors.

Dielectric Classification

Class I Dielectrics

Class I dielectrics are comprised of non-ferroelectric, linear dielectrics, which display the most stable characteristics and have dielectric constants under 150. Class I also includes a subgroup of "extended" temperature compensating ceramics using small additions of ferroelectric oxides (such as $CaTiO_3$ or $SrTiO_3$) that display near-linear and predictable temperature characteristics with dielectric constants ranging up to 500. Both groups are commonly used in circuitry requiring stability of the capacitor because of characteristics such as:

- Little to no aging of the dielectric constant
- Low loss such that the dissipation factor (DF) is less than 0.001 or less than 0.002 for extended temperature compensating ceramics
- Little to no change in capacitance or dielectric loss with voltage or frequency
- Predictable linear behavior with temperature within prescribed tolerances

EIA Standard 198 defines a letter-number-letter code to describe the temperature coefficient of Class I dielectrics as follows:

EIA CLASS I CLASSIFICATION					
Significant Figure of Temperature Coefficient of Capacitance (ppm/°C)		Multiplier		Tolerance of Temperature Coefficient (ppm/°C)	
C	**0.0**	**0**	**-1.0**	**G**	**30**
M	1.0	1	-10	H	60
P	1.5	2	-100	J	120
R	2.2	3	-1000	K	250
S	3.3	4	-10000	L	500
T	4.7	5	+1	M	1000
U	7.5	6	+10	N	2500
		7	+100		
		8	+1000		
		9	+10000		

Table 3. EIA Designations for Class I Dielectrics

The most common Class I dielectric for chip capacitors is the C0G designation (emphasized with red text in Table 3), which is also known as NP0 (negative-positive-zero) in the U.S. military (MIL) specification for its flat temperature coefficient. It has an allowable capacitance change of ±30 ppm/°C over the -55°C to 125°C operational temperature range.

C0G is stable with voltage, has negligible aging, and has a DF at a maximum of 0.15 percent, which is less than the X7R dielectrics described below. When operating at high frequencies, this lower DF means that the power lost in the capacitor is reduced and the component is less prone to overheating. In general, C0G dielectrics have K values of between 20 to 100 and are used to make stable, lower capacitance parts in the picofarad (pF) to nanofarad (nF) region (Figure 20). These devices are typically used for filtering, balancing, and timing circuits.

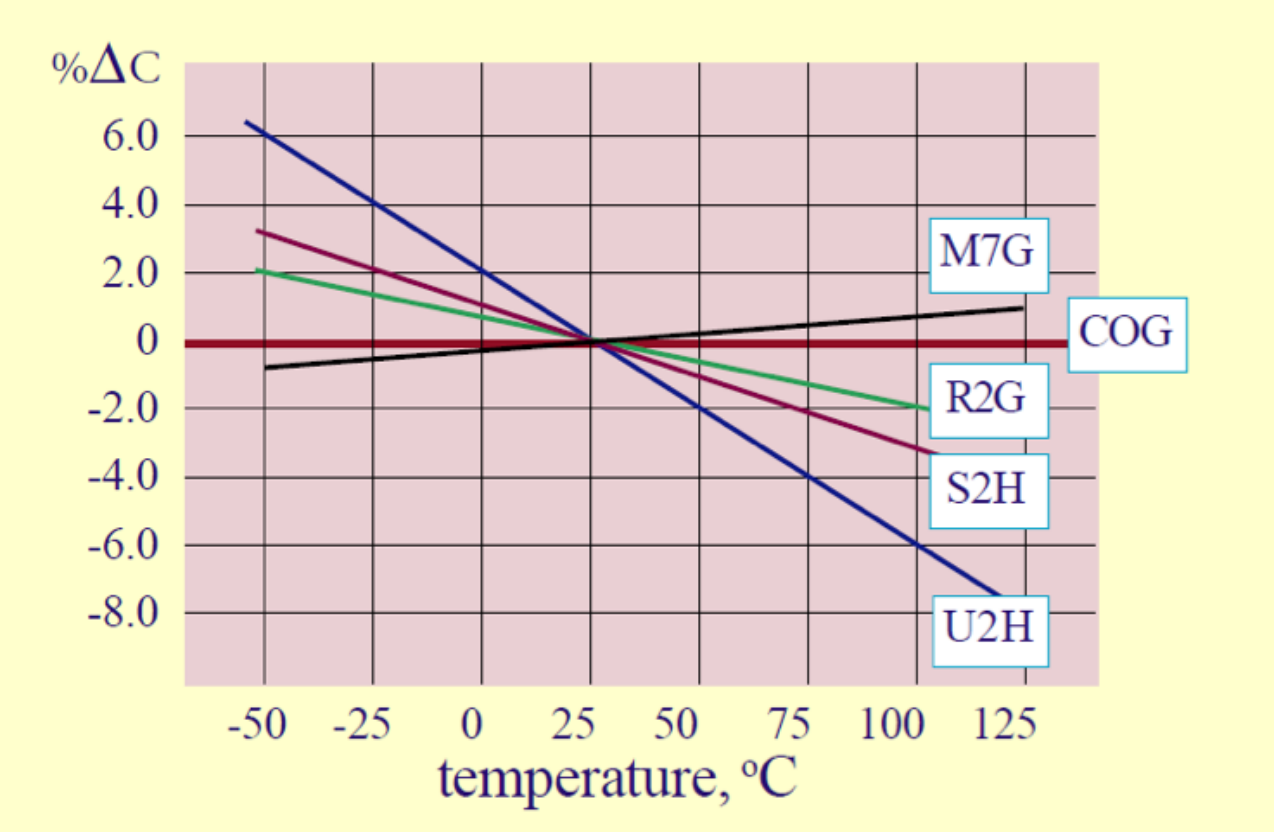


Figure 20. Temperature Coefficients of Linear Dielectrics

Class II Dielectrics

Ferroelectric formulations are categorized as Class II dielectrics. These materials offer much higher dielectric constants than Class I dielectrics, but have less stable properties with regards to temperature, voltage, frequency, and time. The diverse range of properties of the ferroelectric ceramics is split into the following two subgroups, defined by the temperature characteristics:

- **"Stable Mid-K" Class II Dielectrics**—Have a maximum temperature coefficient of ±15 percent from the 25°C reference over the temperature range of -55°C to 125°C. These materials typically have dielectric constants from 600 to 4,000 and meet the EIA X7R characteristics (Table 3).
- **"High K" Class II Dielectrics**—Have temperature coefficients exceeding the X7R requirements. These high K formulations have dielectric constants from 4,000 to 18,000 but with steep temperature coefficients, which is due to the fact that the Curie point is shifted towards room temperature for maximum dielectric constants.

EIA CLASS II CLASSIFICATION					
Minimum Temperature		Maximum Temperature		Capacitance Change Permitted	
X	**-55°C**	4	+65°C	A	±1.0%
Y	-30°C	5	+85°C	B	±1.5%
Z	-10°C	6	+105°C	C	±2.2%
		7	**+125°C**	D	±3.3%
		8	+150°C	E	±4.7%
		9	+200°C	F	±7.5%
				P	±10%
				R	**±15%**
				S	±22%
				T	22%/-33%
				U	+22%/-56%
				V	+22%/-82%

Table 4. EIA Designations for Class II Dielectrics

X7R (emphasized with red text in Table 4) is one of the more commonly used Class II dielectrics. The 'X' and '7' define the lower and upper operational temperature range of -55°C and +125°C, respectively. The 'R' defines the stability within the temperature (±15 percent tolerance). The DF is a maximum of 2.5 percent, and the aging rate for X7R is about 1 to 2 percent per time decade (which means that, at 1 percent aging, 2 percent of the capacitance value will be lost between hour 10 and hour 1,000). X7R has a high K value of around 3,000 and is used for capacitance values in the nF to microfarad (µF) range. With these characteristics, X7R dielectrics are commonly found in energy storage, smoothing, and filtering applications.

The U.S. military specification for ceramic chip capacitors (MIL-C-55681) also falls in the Stable Mid-K subgroup and is designated as "BX." In effect, the BX characteristic is similar to the X7R designation, as long as the voltage coefficient and temperature coefficient combined do not exceed +15% -25 %ΔC. Figure 21 shows some typical Class II temperature coefficient curves.

Next, we will review capacitor test conditions and electrical properties for both ferroelectrics and linear dielectrics, and how these can impact your specific applications.

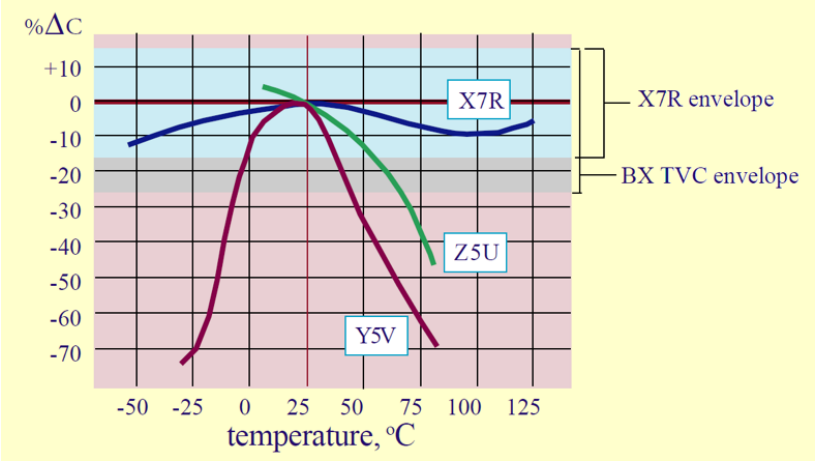


Figure 21. Temperature Coefficients of Ferroelectric Dielectrics

Test Parameters and Electrical Properties

Electrical behavior of ceramic chip capacitors is strongly dependent on test conditions, most notably temperature, voltage, and frequency. This dependence on test parameters is more evident with Class II ferroelectric dielectrics, and negligible, or more easily predictable, with Class I formulations. Therefore, certain industry standards of measurement have been established that give appropriate limits of performance for any given electrical property and dielectric characteristic.

Temperature Dependence

Temperature Coefficient—Capacitance and Temperature Dependence
In general, materials with higher dielectric constants K at 25°C display greater change when the temperature shifts. The temperature coefficient of capacitance (TCC or T.C.) measures the variance of capacitance with temperature and is expressed in units of ppm/°C for Class I capacitors and %ΔC from room temperature measurement for Class II capacitors.

Dielectric Loss and Temperature
Class I dielectrics display only negligible change in DF with temperature over the standard -55°C to 125°C temperature range, whereas Class II dielectrics show a general decrease of DF with temperature, notably at or near the Curie point of the material. At 25°C room temperature, industry standards require for the DF for standard Class I dielectrics (such as C0G-NP0) to not exceed 0.1 percent, whereas the DF for Class II Mid-K dielectrics (such as X7R) should not exceed 2.5 percent and the DF of Class II High-K dielectrics (such as Z5U and Y5V) should not exceed 3.0 percent (Figure 22).

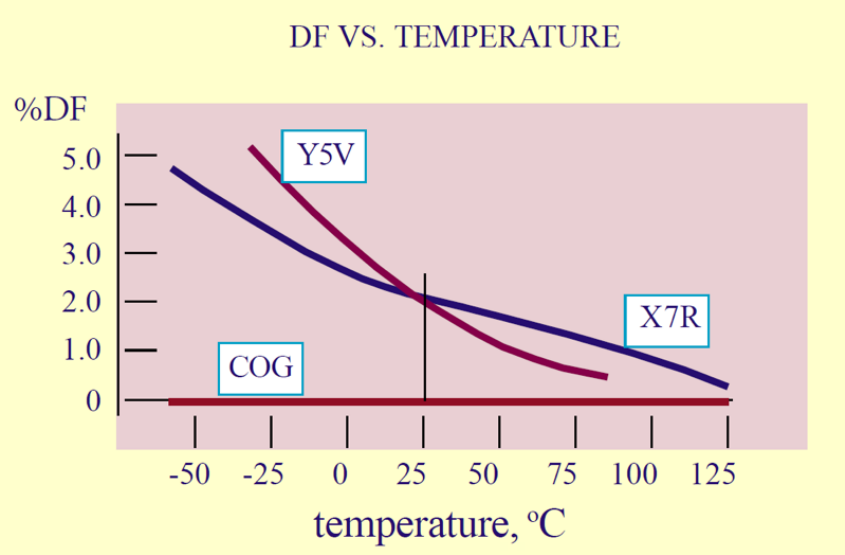


Figure 22. Dielectric Dissipation Factor Curves With Temperature

> **In general, materials with higher dielectric constants K at 25°C display greater change when the temperature shifts.**

Insulation Resistance and Temperature
The capacitance of a capacitor is inversely proportional to its insulation resistance, which is a measure of the capability of a material to withstand leakage of current. Since thermal energy increases the diffusion of charge carriers, leakage of current increases with temperature. Typically, the insulation resistance of most dielectrics at 125°C decreases by a factor of one to two orders of magnitude from the 25°C measurement. Industry standards require that the insulation resistance readings at 125°C exceed 100 ohm-Farad (ΩF).

Dielectric Strength and Temperature
The dielectric strength of insulators is inversely proportional to temperature since heat lowers the intrinsic resistivity of the material. As a general rule, a properly designed capacitor should withstand the normal 25°C dielectric withstanding flash voltage even when the temperature is 125°C.

“The capacitance of a capacitor is inversely proportional to its insulation resistance, which is a measure of the capability of a material to withstand leakage of current.”

DC Voltage Dependence

VDC Coefficient—Capacitance and DC Voltage Dependence
When a DC voltage is applied, all Class II ferroelectric formulations experience an eventual decrease in dielectric constant, and this impact is more severe with dielectrics of higher dielectric constant. The behavior is attributed to a constraint of the DC voltage on the response of the polarizing mechanisms, which give rise to the dielectric constant of the material.

As seen in Figure 23, the expected capacitance changes with increased volts/mil DC bias. The thickness of the individual dielectric layers determines the volts/mil loading of the device during operation. Therefore, capacitors of identical capacitance value and voltage rating may behave quite differently depending on the internal construction of the capacitors.

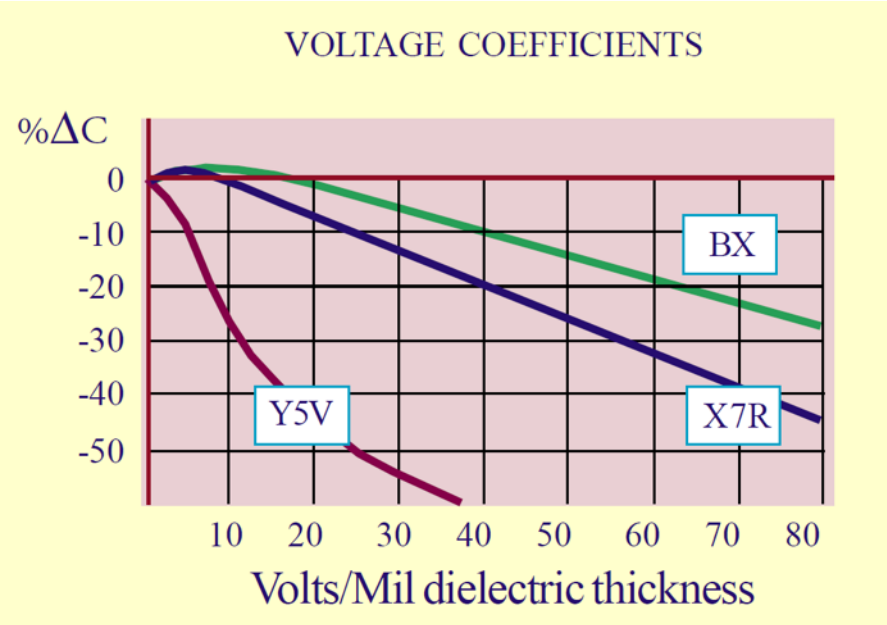


Figure 23. Voltage Coefficients for DC Bias

This effect is of considerable importance in the design of capacitors intended to meet characteristics that require the combined temperature and voltage coefficients (TVC) not exceed a certain ΔC over the operating temperature range, at working voltage. Assuming that a dielectric is available with T.C. characteristics well within the ±15 percent maximum ΔC, the manufacturer usually needs to only be concerned with the negative contribution of the voltage coefficient.

For example, let's consider a X7R capacitor of 0.1 µF that is rated for 50 VDC. This MLCC is constructed with 30 layers that are 1.5 mm thick, which means the dielectric layers only experience 33 volts/mm when operating at 50 VDC. Therefore, according to Figure 23, the VC is only -15 percent. If the T.C. of the dielectric is ±7%ΔC and the VC is -15%ΔC, then the maximum TVC is +7%-22% ΔC.

> **Class II dielectrics experience an accelerated aging effect when stressed by DC voltage, even at room temperature, and the effect is even stronger at higher voltages and with dielectrics with elevated dielectric constants.**

Voltage Conditioning and Aging
Class II dielectrics experience an accelerated aging effect when stressed by DC voltage, even at room temperature, and the effect is even stronger at higher voltages and with dielectrics with elevated dielectric constants. When manufacturing close tolerance (±5 percent) Mid-K dielectrics, or high voltage units, the product is usually reheated after IR or dielectric withstanding voltage testing to maintain capacitance tolerance and establish a fresh aging cycle. X7R units may derate as much as 3 percent in capacitance after DC withstanding voltage testing at 300 volts/mil.

Dissipation Factor and DC Voltage
Class II dielectrics experience a decrease in dielectric loss with increasing voltage. In fact, the DF may be reduced by a factor of 75 percent at 100 volts/mil bias for X7R dielectrics.

AC Voltage Dependence

AC Voltage Coefficient—Capacitance and AC Voltage Dependence
With Class II capacitors, the dielectric constant always increases with the AC test voltage, with higher K dielectrics responding more readily, until some threshold voltage value is reached where the effect reverses. Class I dielectrics, operating in the paraelectric state, display negligible or only limited response to the AC bias.

Industry standards specify a test voltage of 1.0 ±0.2 Vrms for all dielectrics, with the exception of some High-K less stable Class II bodies that are typically specified by manufacturers at 0.1 or 0.5 Vrms. Therefore, application of these materials at other volta ges presents correlation problems, even at low voltage stress (under 5 Vrms/mil) as seen in Figure 24. As with the DC voltage coefficient, the situation is further complicated by the added variable of capacitor design (i.e., dielectric thickness of the individual layers).

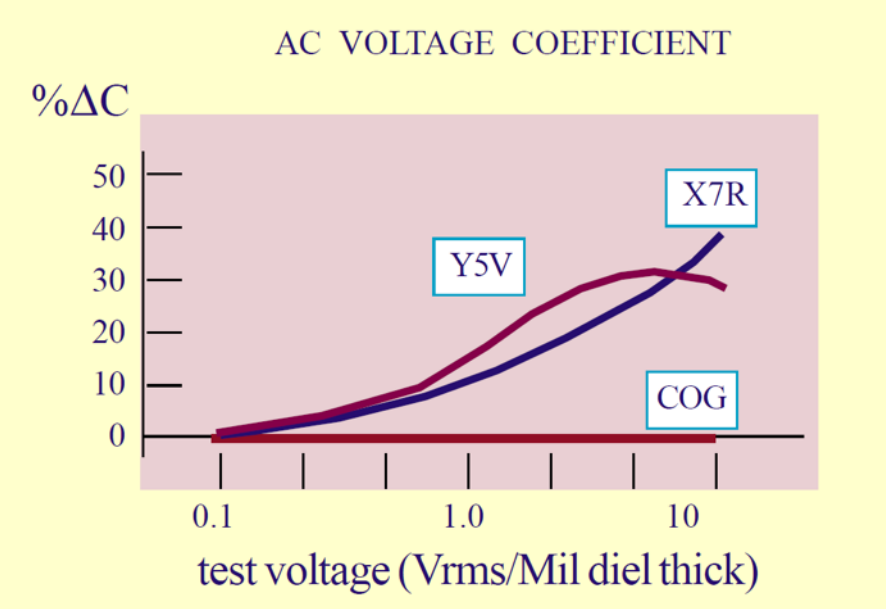


Figure 24. AC Voltage Coefficients

Dissipation Factor and AC Voltage

The increase of dielectric constant with AC test voltage is accompanied by a marked increase in the dissipation factor, as illustrated in Figure 25. Since MLCCs are constructed with thin dielectric layers, they are not ideal for use circuitry with large AC voltage and high current, as dielectric losses become quite significant between 5 and 20 Vrms/mil stress.

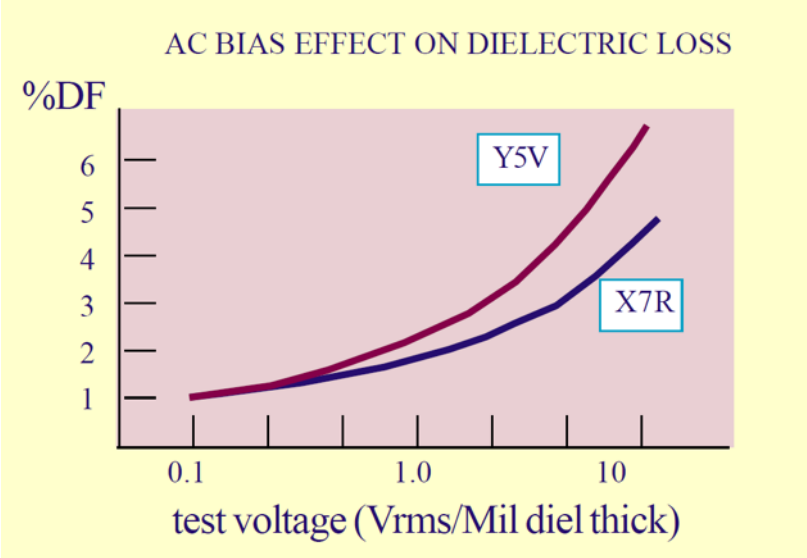


Figure 25. AC Bias Effect on Dielectric Loss

The increase of dielectric constant with AC test voltage is accompanied by a marked increase in the dissipation factor.

Frequency Dependence

Previously, we discussed the close interrelationship of frequency and dielectric polarization and dielectric loss. Essentially, increased frequency of an applied field results in a decrease of the measured capacitance value. Some polarizing processes have slower reaction times that cannot keep up with high frequency polarity reversals of the field, resulting in decreased dielectric constant and increased dielectric loss.

These effects are common to all the dielectric groups but are more predominant in the ferroelectric formulations which display large ionic polarization. Typical curves for capacitance and dissipation factor versus frequency are illustrated in Figures 26 and 27.

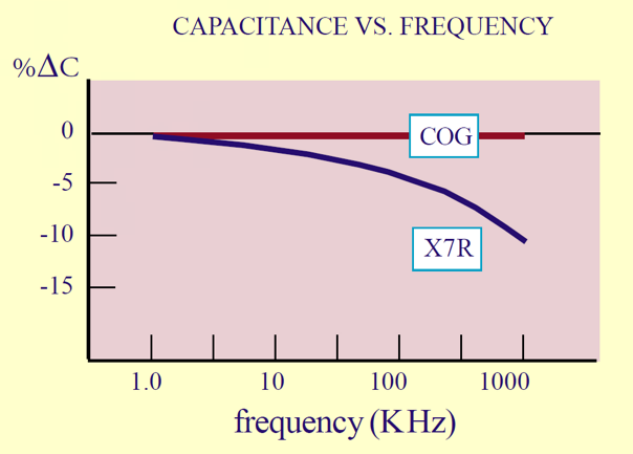


Figure 26. Capacitance vs. Frequency

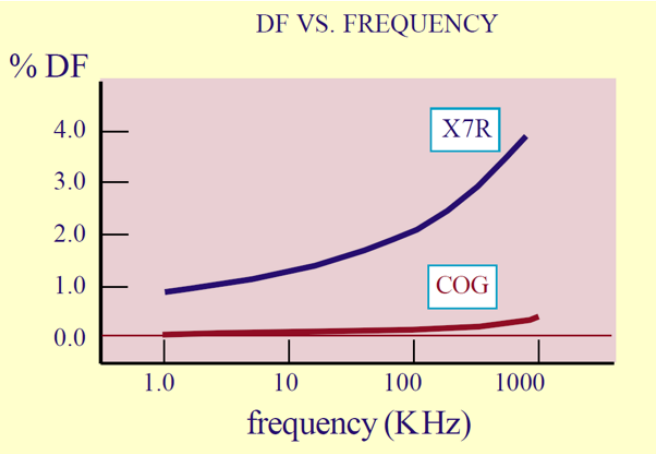


Figure 27. Dissipation Factor vs. Frequency

> **Essentially, increased frequency of an applied field results in a decrease of the measured capacitance value.**

Aging and Time Dependence

As previously discussed, ferroelectric dielectrics exhibit aging, where capacitance loss occurs as the ions in the crystal lattice shift and stabilize to positions of lower potential energy. Restraints on the percentage capacitance loss per decade hour aging rates are usually specified by users of chip capacitors.

X7R is expected to age less than 2.5 percent/decade hour, and most dielectrics within this characteristic typically have aging rates from 0.8 to 2.0 percent per decade hour. The High-K aging specification is more liberal by necessity, for example, an aging rate of 5 percent per decade hour is considered normal. Many of the Class II dielectrics may also display aging of the dissipation factor, an effect more predominant with High-K formulations.

Industry Test Standards Overview

Beyond understanding test parameters for dielectrics, it is also important to understand the industry standards set by both the EIA and mil/aero industry. Chip capacitor test parameters, performance specifications, and quality conformance requirements are outlined in the EIA 198 and MIL-C-55681 specifications. Table 5 shows a summary of electrical specifications for popular Class I and Class II dielectrics.

	COG or NPO EIA 198, MIL-C-55681	BX MIL-C-55681	X7R EIA 198	Z5U EIA 198	Y5V EIA 198
Oper. Temp. Range	-55°C to 125°C	-55°C to 125°C	-55°C to 125°C	10°C to 85°C	-30°C to 85°C
Temp. Coefficient %ΔC Max., 0 Bias	0 +/- 30 ppm/°C	+/- 15%	+/- 15%	+22% -56%	+22% -82%
Temp-Volt Coeff. %ΔC Max., @ Vdc	0 +/- 30 ppm/°C	+15% -25%	N/A	N/A	N/A
Dissipation Factor, @ 25°C	0.10% Max.	2.5% Max.	2.5% Max.	3.0% Max.	5.0% Max.
Insulation R @ Vdc, 25°C	>100GΩ or >1000ΩF	>100GΩ or >1000ΩF	>100GΩ or >1000ΩF	>10GΩ or >100ΩF	>10GΩ or >100ΩF
Insulation R @ Vdc, 125°C	>10GΩ or >100ΩF	>10GΩ or >100ΩF	>10GΩ or >100ΩF	N/A	N/A
Dielectric Test Voltage, 25°C	250% WVdc	250% WVdc	250% WVdc	250% WVdc	250% WVdc
Aging Rate, Max %ΔC/decade	0%	-2.0%	-2.5%	-3.0%	-5.0%
Test Frequency, 25°C	<100 pF, 1.0 MHz >100 pF, 1.0 KHz	1.0 KHz	1.0 KHz	1.0 KHz	1.0 KHz
Test Voltage, 25°C	1.0 +/- 0.2 Vrms	1.0 +/- 0.2 Vrms	1.0 +/- 0.2 Vrms	0.5 +/- 0.2 Vrms	0.5 +/- 0.2 Vrms

Table 5. Electrical Specifications for Class I and II Dielectrics (EIA 198 and MIL-C-55681)*

*Note: The dielectric withstanding test voltage shown in the table applies to voltage ratings for 200V or less. Typically, the following test voltages apply for varied ratings:

16V to 200V: 250 percent WVdc
>200V <500V: 150 percent WVdc, or 500V (whichever is greater)
<500V: 120 percent WVdc, or 750V (whichever is greater)

Chip capacitor test parameters, performance specifications, and quality conformance requirements are outlined in the EIA 198 and MIL-C-55681 specs.

Relevant EIA and MIL test methods and quality conformance requirements (most commonly applicable to MLC capacitors) are given in Table 6.

Specification	Test Category	MIL Method Number	EIA-198-1-E Method	Test Description
EIA-198-1-E MIL-C-55681: MIL-STD-202F (MIL-STD-883E)	Environmental	103B 104A (1002) 106F (1004.7) 107G (1011.9) 108A (1010.7)	205 203 204 202 201	Humidity Immersion Moisture Resistance Thermal Shock Life (@ elevated Temp.) Temperature Cycling
EIA-198-1-E MIL-C-55681: MIL-STD-202F (MIL-STD-883E)	Physical	204D 208H (2003.7) 210E 211A 212A 213B (2002.3) 215J (2001.2)	304 301 302 303 305 210 306(EIA-469-C)	Vibration Solderability Resistance to Solder Heat Termal Strength Acceleration Shock Resistance to Solvents Constant Acceleration Destructive Physical Analysis
EIA-198-1-E MIL-C-55681: MIL-STD-202F (MIL-STD-883E) MIL-PRF-49467A	Electrical	301 302 (1003) 305 306 Appendix B	103 104 101 102 105	Dielectric Withstanding Voltage Insulation Resistance Capacitance and DF Quality Factor Voltage-Temp. Cap Coefficient Partial Discharge (High Voltage)

Table 6. General Testing and Quality Conformance Specifications for Chip Capacitors

High Reliability Testing

Determining Capacitor Reliability

Product durability and accelerated life cycle testing are methods used to determine the reliability of a product before release. By subjecting the capacitor to elevated conditions far beyond its normal operational ranges, the goal is to discover any defects or points of failure to better inform customers about the limitations of the unit.

> **Chip capacitors destined for high-reliability testing are often designed with an added margin of safety, namely maximization of the dielectric thickness, and tested extensively for electrical properties prior to burn-in.**

Burn-In Testing

Dielectric formulations and chip capacitors are often tested for reliability under voltage and temperature for specified time periods, a process referred to as burn-in or voltage conditioning. The specifications applicable to burn-in of MLCCs are MIL-C-55681, MIL-C-123, and MIL-C-49467. Burn-in may also be performed to customer specifications. Typically, a test voltage is used that is twice the working voltage rating of the device, at 85°C or 125°C, for a duration of 96, 100, or 168 hours of test time.

Burn-in is accomplished by loading the units in a fixture, usually a printed circuit board (PCB) that connects to a power supply with access to the rear wall of a standard oven. Units are monitored for current leakage under voltage and temperature stress, either individually or in tandem, with measurement of leakage from a group of a hundred units typically. Tandem testing is more rapid and used to mass-produce burned-in product. Sophisticated test equipment is used with automated data monitoring to record the location and time of test cycle failures.

Chip capacitors destined for high-reliability testing are often designed with an added margin of safety, namely maximization of the dielectric thickness, and tested extensively for electrical properties prior to burn-in (e.g., capacitance, dissipation factor, and insulation resistance). This pre-test data is compared to the post burn-in data to evaluate the reliability of the components.

Failure Modes for Burn-In Testing

Capacitors which fail burn-in usually lose resistivity at the elevated temperature and voltage, either catastrophically or gradually with time, resulting in insulation resistance rejects. The failure rate is usually inversely proportional with time, such that more failures are observed earlier in the test cycle.

However, excellent electrical properties at 25°C may not guarantee good performance during life cycle testing for the following reasons:

- Poor dielectric properties—Ceramic dielectrics with elevated insulation resistance at room temperature may experience excessive loss of resistivity at 125°C due to improper formulation. This causes the charge carriers to become mobile and develop a leakage current, decreasing the insulation resistance below specifications.
- Poor microstructure—Voids, cracks, or delaminations within the chip structure undermine the intrinsic

resistivity of the material, providing leakage paths conducive to failure. Experience has shown that despite rigorous testing, units with delaminations may still perform adequately, while failures may be observed in units with apparent "excellent" microstructure. This is because defects that happen to straddle the electrode array are more conducive to eventual degradation under voltage and temperature.

> **Capacitors which fail burn-in usually lose resistivity at the elevated temperature and voltage, either catastrophically or gradually with time.**

A second failure mode independent of the above reasons is degradation of the capacitance value and/or DF of the chip capacitor, when the post burn-in data does not correlate well to the original test data.

Class I non-ferroelectric dielectrics do not exhibit capacitance aging with time, temperature, or voltage. Therefore, any burn-in induced capacitance change in Class I chips is associated with mechanical failure, such as cracking, which isolates electrode layers. On the other hand, class II ferroelectric dielectrics, may display capacitance and DF variations after burn-in without mechanical failure, since these dielectrics are time-, temperature-, and voltage-dependent.

Most notably, the accelerated aging of the dielectric constant under burn-in conditions must be considered (e.g., in comparison to pre burn-in data performed on de-aged units) for proper interpretation of results. Units under test may be exposed to the following three different aging scenarios, depending on the method used to terminate the life test:

- Procedure 1—The voltage is removed while the units are at temperature, and temperature is maintained with no bias for a minimum of one hour. Under this condition, total de-aging of capacitors occurs, and units will display minimal (positive or negative) capacitance change with respect to the original pre-burn-in values.
- Procedure 2—Capacitors remain under DC bias while the oven is permitted to cool to room temperature. This in effect is a voltage conditioning process and the units will therefore age with respect to the original test data (e.g., -7.0% ΔC).
- Procedure 3: The voltage is removed at the burn-in temperature, and the units subsequently taken from the oven and allowed to air cool to room temperature. In this case, the units do not fully age during the cooling cycle as in procedure 2, nor do they totally de-age as in procedure 1. The components thus experience a partial aging only (e.g., -3.5% ΔC).

The %ΔC values given as examples for the post burn-in data above are typical of some Mid-K Class II dielectrics. High-K less stable dielectrics may experience more radical capacitance changes, as these materials have a typical aging rate of 5 percent per decade hour, which is three times the average rate of X7R formulations. These considerations clearly indicate that procedure 1 only should be followed for termination of the life test for proper evaluation of performance of Class II dielectrics.

In addition to burn-in, high-reliability testing often involves other performance tests per MIL-C-55681 or to customer specifications. The most common of these additional tests are dielectric withstanding voltage and insulation resistance at elevated temperature, voltage-temperature limits, thermal shock, solderability, and solder leach resistance of the chip capacitor termination. In addition, strict visual and mechanical examination of the product may be required, including destructive physical analysis (DPA). The various group categories of high-reliability testing applicable to MIL specifications are outlined in Table 7. Any or all of the group tests may be specified by customers requiring a high-reliability product.

Specification	MIL-C-55681	MIL-C-123B
GROUP A	Voltage Conditioning IR @ Elevated Temperature Visual & Mechanical Inspection ESR, when Specified Solderability	Thermal Shock Voltage Conditioning Visual & Mechanical Inspection, Destructive Physical Analysis
Specification	**MIL-PRF-49467A (High Voltage)**	**MIL-PRF-39014F (Leaded Devices)**
GROUP A	Thermal Shock Voltage Conditioning Partial Discharge Radiographic Inspection Mechanical Examination Visual Examination Solderability	Thermal Shock Voltage Conditioning Radiographic Inspection Mechanical Examination Visual Examination Solderability
GROUP B GROUP C	Environmental and Life Tests performed for qualification, or to attain Established Reliability, applicable to any specification, if required.	

Table 7. High-Reliability Test Procedures

High-K less stable dielectrics may experience more radical capacitance changes, as these materials have a typical aging rate of 5 percent per decade hour, which is three times the average rate of X7R formulations.

Visual Standards For Chip Capacitors

External Visual Standards

In addition to meeting strict industry standards and passing rigorous electronic testing, MLCCs must possess fine workmanship and physical integrity. Thus, visual inspection of the product is performed at 20X magnification to check for defects in the capacitor body and end metallization. Visual standards are detailed in MIL-C-123B, Appendix C, and manufacturers typically inspect only sample quantities in accordance with MIL STD 105, Level II, 0.65. Acceptance or rejection of standard production lots is based on various defective criteria, as listed in Table 8 and depicted in Figure 28.

Major Defects:

1. Cracks, blisters, raised surfaces or delaminations in the capacitor body.
2. Chips or voids in the capacitor body which exceed .003" (.08mm), or which expose internal electrodes.
3. Foreign debris bonded to the chip surface, which exceeds .005" (.13mm)
4. Miscutsof the capacitor edge which penetrate the surface by more than .005" (.13mm), or expose internal electrodes. Flared edges.
5. Termination defects:
   - Voids in the termination which expose eletrodes.
   - Voids in the termination exceeding .005" (.13mm).
   - Exposed metallized edges which exceed 10% of edge dimension.
   - Bare corners on metallized ends.

Minor Defects:

1. Minor irregular cuts of sides or corners
2. Foreign debris on capacitor suface not exceeding .005" (.13mm).
3. Termination Defects:
   - Voids in metallization less than .005" (.13mm).
   - Exposed metallized edges which do not exceed 10% of edge dimension.
   - Poor marking (if applicable)

Table 8. Typical Criteria for Visual Defects

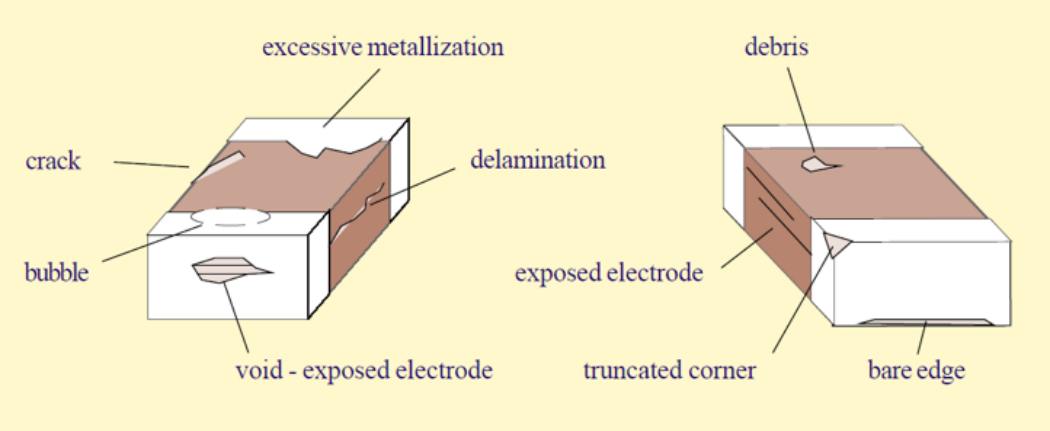


Figure 28. Visual Defects

Internal Microstructure Standards

In addition to the external visual characteristics, quality standards for internal microstructure of the chip capacitor are also applicable, as viewed on polished cross sections of capacitor samples. Units are sectioned along the long and short dimension of the capacitor to provide two edge views of the internal electrodes and terminals.

Although any degree of internal defect is considered undesirable, the fact remains that these types of defects can occur occasionally in different degrees of severity. Typically, delaminations, internal voids, cracks, and other irregularities (Figure 29) are classified based on their severity and are considered to constitute defects if they exceed the criteria based on EIA 469.

Delaminations
A delamination is a separation of the structural layers of the capacitor, in the form of a planar cavity, between the electrode and ceramic or within the dielectric itself. Any delamination that can be considered to be detrimental to the electrical and mechanical integrity of the capacitor is classified as a defect, and generally involves the following:

- Any delamination in the active (electrode overlap) area, longer than 20 percent of the electrode length, or exceeding .010” (.254 mm), whichever is greater
- Any delamination greater than .005” (.127 mm), located within the electrode overlap area, and associated with displacement of adjacent electrodes and reduction of these dielectric layers by more than 50 percent of their thickness
- A delamination that exceeds 50 percent of the margin between the termination and electrodes of opposite polarity
- Two or more delaminations exceeding .010” that overlap in the active electrode area, in adjacent layers

“Although any degree of internal defect is considered undesirable, the fact remains that these types of defects can occur occasionally in different degrees of severity.”

Voids
Any void that can be considered detrimental to the electrical and physical integrity of the capacitor is classified as a defect, and generally involves the following:

- A void between electrodes of opposite polarity that reduces the dielectric thickness by more than 50 percent
- A void in the cover plate of the capacitor that reduces the cover thickness to less than .003” (.076 mm), or less than the active dielectric thickness
- A void or bubble in the termination, not contacting the dielectric surface, that exceeds 30 percent of the chip end dimension
- A void or bubble in the termination, contacting the dielectric, that exceeds .020” (.508 mm)

Cracks
Any crack that can be considered detrimental to the electrical and physical integrity of the capacitor is classified as a defect, and generally involves the following:

- Any crack connecting any two electrodes
- Any crack connecting an electrode to any exterior surface of the chip, or to a termination
- Cracks extending from the termination metal band into the interior of the chip (also known as termination stress cracks)

Non-Uniformities
Irregularities in the construction of the chip capacitor do not necessarily affect the mechanical or electrical integrity of the device, but may be of concern in high-reliability applications. The following is a compilation of structural irregularities according to the EIA 469:

- A side or end margin of dimension less than .003" (.076 mm) between 90 percent or more of the electrodes and the exterior dielectric surface
- Ceramic cover plate thickness less than the dielectric thickness between adjacent electrodes
- Variations in the active dielectric layers that result in areas with less than 50 percent of the nominal dielectric thickness
- Thick electrode depositions, exceeding 2.5 times the average electrode thickness, and extending over 50 percent of the electrode length
- Thick electrode deposition, extending over .005" (.127 mm), that also reduces the adjacent dielectric layer thickness by more than 30 percent

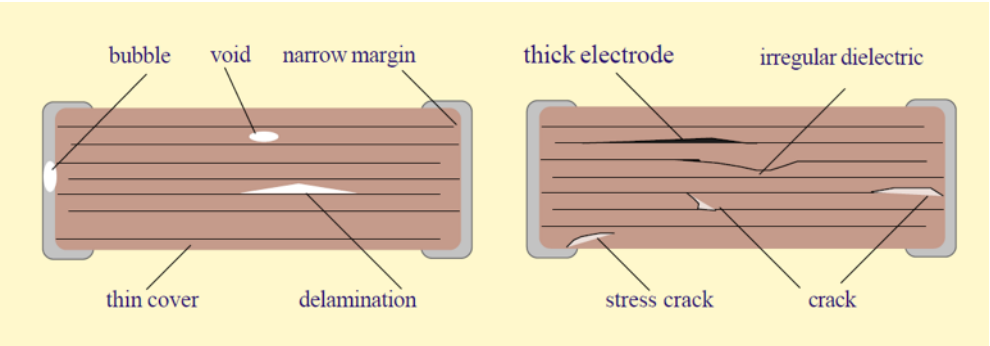


Figure 29. Microstructure Defects

Sample Preparation Defects
A variety of imperfections observed on sectioned specimens can arise due to the method of sample preparation and must be identified to preclude an erroneous interpretation of results. Subtle observations and precautions can be followed to positively segregate preparation problems from actual defects.

Irregularities in the construction of the chip capacitor do not necessarily affect the mechanical or electrical integrity of the device, but may be of concern in high-reliability applications.

First, it is essential that the specimen be observed prior to mounting in a section to determine if any obvious mechanical flaws are present. Usually this is accompanied by inspection of basic electrical properties. Second, units must be rigidly encapsulated with non-shrinking, and hence stress-free, resin, followed by grinding and polishing with fine grit abrasives under controlled pressure to avoid cracking. Sections must be polished to remove all vestiges of the rough cuts used to reduce the specimen and then cleaned thoroughly before observation. This procedure will minimize the occurrence of most sectioning-induced defects (Figure 30).

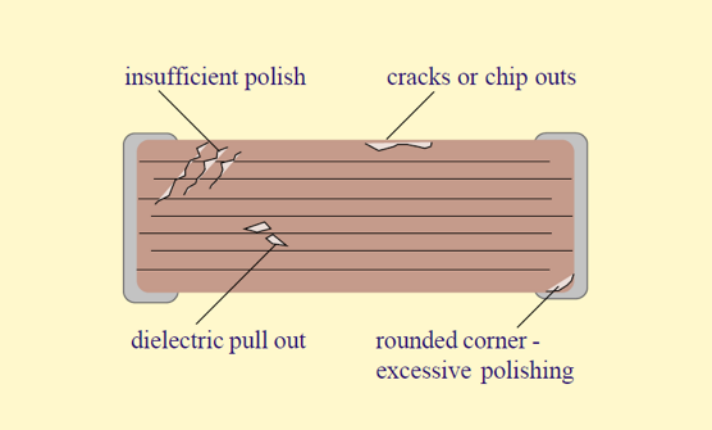


Figure 30. Sample preparation defects

> **It is essential that the specimen be observed prior to mounting in a section to determine if any obvious mechanical flaws are present.**

The following criteria are used to attribute defects to sectioning methods:

- Void defects form linear patterns and are induced by grit pulling material out of the ceramic during grinding, hence more polishing is required. Note that voids forming a line parallel to the layered structure of the device, a so-called “knit line,” may not fall into this category.
- Large voids are present, with virtually no distortion of the electrode pattern or of adjacent dielectric layers. The correctness of the structure around these voids is indicative as to their absence in the original unsectioned unit; thermal processing would otherwise result in collapse of the electrode and/or distortion of layers around these voids. Such defects are caused by excessive pullout during grinding, particularly in the area between electrode layers, where there is minimal dielectric layer to layer bonding.
- Units exhibit cover sheet cracks and/or separation of the ceramic cover sheet from the electrode array, yet these were not evident on usual examination of the device prior to sectioning. These defects arise due to insufficient support in the encapsulant and/or excessive grinding methods. Such cracks may also appear parallel to the end terminations, as the termination to ceramic interface is mechanically weaker. Measurements of capacitance, DF, insulation resistance, and termination pull strength can be used to confirm the absence of this defect in unsectioned product.
- Excessive polishing will round corners and edges of the section, resulting in depth-of-field distortions on observation, as well as difficulty with illumination. “Defects” which appear under these conditions may be nonexistent and should be disregarded.

Evaluation of visual and microstructure quality of chip capacitors is subjective, and difficulties arise in correlating opinions between observers, especially when considering the minor category of defects described above. In addition, dissimilar images can occur when viewing product under differing light sources on a microscope. For example, fluorescent lighting has been found to be superior over incandescent light in highlighting defects. The acceptance or rejection of capacitors with any visual or microstructure defects is usually specified or determined by the chip user, based on the application of the product. High-reliability or high-voltage units must meet the most stringent standards.

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Chip Attachment and Termination Guidelines

Now that we've reviewed the importance of the physical integrity of a capacitor, which is determined through visual inspection, let's discuss the different chip capacitor attachment methods, thermal properties, and performance specifications to consider.

Traditionally, leaded capacitors were used in high-volume PCBs, such that the components were assembled or "stuffed" into plated through holes on P.C. boards. Nowadays, MLCCs are often sold as chip (or leadless) components that can be surface mounted to high-density boards using high-speed automation. However, variables affecting attachment of chips to substrates are of increasing importance. The inherent mismatch of thermal and physical properties of the components to the substrates and solders is intensified by the use of chip components directly bonded to the substrate material.

Chip Capacitor Attachment Methods

Chip bonding to substrates can be categorized into the following two general classes:

1. Methods involving solder
2. Methods involving other bonds, such as epoxies and wire bonds (thermal-compression and ultrasonic bonding)

#1 Soldering
Solder attachment can be accomplished in a variety of ways, including:

- Hand soldering of chips to substrate pads
- Reflow of pre-tinned capacitors on pre-tinned substrate pads
- Reflow of capacitors on substrate pads covered with a solder preform or with screened on solder paste
- Wave soldering of chips and substrate (with chips held in position with nonconductive epoxy), which allows units to be attached to both sides of the substrate for greater packing density

A common method used in the surface mount industry is the solder paste reflow technique, and involves the following basic steps:

1. The capacitors and substrate are prepared by cleaning with a mild solvent and pre-fluxing
2. The substrate is pre-tinned with solder using solder paste, molten solder dipping, or solder preforms
3. The capacitor-substrate assembly is heated to the solder flow point temperature to form a well-formed solder fillet
4. The assembled substrate is cleaned with a mild solvent (usually ultrasonically) to remove flux residues

A common method used in the surface mount industry is the solder paste reflow technique.

The advent of high component density circuits, which utilize surface mount technology, has resulted in the need for more thermal efficient and reliable soldering methods. Surface mount components are attached to the substrate by pick-and-place machines, and held in place by epoxy or solder paste for subsequent processing, which may involve any of the following:

- **Infrared (IR) Solder Reflow**—This method was briefly described above and has the advantage of having precise temperature profiles. This allows for good control of the many parameters of the circuit assembly, including volatilization of solvents, activation of fluxes, solder reflow and wetting time, and uniform and gradual cooling.
- **IR Heat Transfer**—This method is by direct radiation, and different, specific profiles need to be established for variations in board type and configuration. Generally, IR profiles spend several minutes at temperatures below 100°C to volatize the solvents, increase the temperature to just below the solder melting point, and then rapidly spike to 30°C to attain solder wetting and the formation of clean fillets.
- **Vapor Phase Reflow**—This method is based on rapid and thermally efficient transfer of heat from hot vapors to the hybrid assembly. The advantage of this system is that total immersion of the circuit in the hot vapor provides a more uniform heat transfer for reflowing the solder. However, problems may arise with sudden outgassing of paste constituents and thermal shocking of components.
- **Solder Wave**—This technique contrasts with the above in that soldering is accomplished by direct contact of the hybrid assembly to molten solder. The circuit is transported through programmed flux, preheat, soldering, and cooling cycles. Total immersion in flux and molten solder is attained by pumping them through a fixture to create a constantly flowing crest or "wave" of sufficient height to cover the circuit in its entirety as it is conveyed through. Controlled heating and cooling cycles are required to minimize thermal stresses within the components and bonds.

The objective of any solder attachment system is the same: to attain clean and smooth solder joints with no bridging or open areas and without physical defects. Not all these parameters are solder processing dependent, since certain defects can be attributed to component or circuit faults or selection of materials. The degree of bond strength of the components to the board is also dependent on the quality of the chip termination, its own intrinsic strength, solderability, and resistance to solder leach, as well as the selection of solder.

> **The objective of any solder attachment system is the same: to attain clean and smooth solder joints with no bridging or open areas and without physical defects.**

#2 Epoxy Bonding

Nonconductive thermosetting epoxies are utilized to affix the capacitor body to the substrate, in preparation for secondary electrical connection, either by soldering (solder reflow or solder wave) or by wire bonding (ultrasonic or thermal-compression bonding). An electrical mechanical bond, analogous to soldering of chips, can be achieved by using conductive epoxies, which contain metal powders of silver, copper or aluminum. Epoxies require a low temperature cure in the range of 25°C to 150°C.

#3 Wire Bonding

Wire bonding methods involve welding of very thin gold or aluminum wires to components to affect an electrical connection; physical attachment of the capacitor body to the substrate must be made by other means, such as epoxy bonding. The wire bond to the chip metallization or substrate pad is attained with heat and pressure applied to the fine diameter wire tip. Localized heat at the bond is applied from an external source, as in thermal-compression bonding or ultrasonic bonding. In both cases, the heat and pressure result in intermetallic mingling of the wire and host material, effecting a bond.

Thermal Properties of Chip Capacitors

Chip attachment methods invariably involve thermal cycling of the component. The expansion characteristics of the chip and substrate and the mechanical properties of the bonding medium result in residual stresses that affect the reliability of the bonded chip.

Chip capacitors can tolerate relatively high temperatures, by virtue of their processing, which typically involves a 1,100°C to 1,200°C firing of the dielectric body, followed with a second firing of the end metallization at approximately 850°C. Chips therefore could be cycled to as high as 850°C with no detrimental effect on the devices, provided the process does not expose the product to sudden or nonuniform temperature changes, which can cause thermal shock failure. Capacitors with nickel barrier terminations, which have a solder coat over the nickel, (or solder coated terminations) are restricted to the reflow temperature of the solder.

“The expansion characteristics of the chip and substrate and the mechanical properties of the bonding medium result in residual stresses that affect the reliability of the bonded chip.”

Temperature cycling causes a change in the mean interatomic spacing of the atoms in the crystal lattice due to variations in thermal energy. The characteristic dimensional change of materials with temperature is a function of temperature, and if the dimensional changes caused by temperature cycling are not uniform, the resultant differential strains cause stresses within the material. These stresses are significant in ceramic materials, which, unlike metals, lack ductility to relieve the stress. Heating of a material causes a positive expansion, resulting in compressive stress. Conversely, cooling results in tensile forces as the material attempts to contract.

As ceramics are characteristically weaker under tensile load, it follows that the type of temperature change, i.e. heating or cooling, as well as the rate, uniformity and degree of change are critical. Thermal cycling of chip capacitors therefore involves the following general precautions:

- The rate of heating must be uniform and controlled to preclude the occurrence of differential strains in the chip, as is accomplished in a reflow furnace. Other soldering methods, such as hand or wave soldering, should be preceded with a preheat cycle to bring the components to the solder flow temperature gradually. Although heating generally produces the more benign compressive stresses in the ceramic body, it should be noted that the more heat conductive chip end metallizations heat preferentially, i.e., the chip ends expand more rapidly than the main body of the chip, resulting in tensile stresses between the body and metallized ends.
- Chip capacitors are even more vulnerable to failure during the cooling cycle, as negative temperature gradients cause primarily tensile stress. Cooling must therefore be gradual and uniform, with no localized forced cooling or contact of the chip with any efficient heat sink.

The effects of capacitor geometry are self-evident; thermal gradients and resultant stresses are directly proportional to chip mass; hence, larger units are more susceptible to thermal shock than smaller devices. Also, the contribution of preferential heat conduction of end terminations to undesirable stresses increases with larger or longer chips, as more mass is available to maintain the thermal gradients.

Without mechanical restriction, thermally induced stresses are released once the capacitor attains a steady state condition, at any given temperature. Capacitors bonded to substrates, however, will retain some stress, due primarily to the mismatch of expansion of the component to the substrate. The residual stress on the chip is also influenced by the ductility, and hence the ability of the bonding medium to relieve the stress. Unfortunately, the thermal expansions of chip capacitors differ significantly from those of substrate materials.

Chips bonded to alumina therefore will retain a tensile stress, as the expansion coefficient of the dielectric material exceeds that of the substrate. On cooling, the chip capacitor will attempt to shrink more than the substrate but is restrained from doing so by the substrate material and solder or epoxy bond. Chips bonded to PCB will retain a compressive stress, as the substrate material attempts to shrink more than the chip. In either case, a shear stress is incorporated into the bond medium; therefore, the reliability of the bond is greatly dependent on the load bearing capability of the bonding material.

Selection of Solder

Solders are the most common bonding alloys used in capacitor attachment. “Low temperature” solders with flow points under 250°C are generally tin-lead alloys, with or without silver additions. “High temperature” solders with flow points of 260°C to 370°C are based on high lead content alloyed with silver and/or tin or based on gold alloyed with germanium or tin.

Solders are selected based on the assembly temperature restrictions of the circuit, the hardness or ductility of the alloy, and the comparability of the solder to the chip termination and substrate conductor composition. Common solder types, flow points, and hardness are tabulated in Table 9.

Solder Type	Flow Point C	Brinell Hardness
Sn63 (63Sn, 37Pb)	183	30
Sn60 (60Sn, 40Pb)	189	28
Sn62 (62Sn, 36Pb, 2Ag)	189	33
Sn50 (50Sn, 50Pb)	212	24
95Sn, 5Ag	240	22
80Au, 20Sn	280	115
Sn5 (95Pb, 5Sn)	312	15
88Au, 12Ge	356	107
95Pb, 5Ag	360	12

Table 9. Common Bonding Alloys

“Solders are selected based on the assembly temperature restrictions of the circuit, the hardness or ductility of the alloy, and the comparability of the solder to the chip termination and substrate conductor composition.”

The following considerations should be made when selecting the appropriate solder:

#1 Solder Leach
At the solder flow temperature, tin-lead alloys absorb silver or gold from the chip termination and/or the substrate pad. This effect is minimized by using solders which contain some percentage of silver and by limiting the time at reflow temperature to the minimum required to obtain good wetting and a well-rounded fillet. Excursion of temperature above the flow point of the solder also need to be avoided, as the leaching rate increases rapidly with temperature. The leaching effect is cumulative; repeated reflow of the solder during processing of the circuit will aggravate the problem.

Capacitor termination alloys and geometry are designed to reduce the leaching effects of solders. Termination materials have evolved from pure silver to silver-palladium alloys, typically 80Ag-20Pd, as the palladium inhibits silver leaching. Leaching, if it occurs, is predominant at the corners and edges of the chip termination, where the termination alloy is thinnest. This effect is minimized by the chip manufacturer by rounding of the corners and edges of the chip with a tumbling process before terminations are applied to obtain a more uniform thickness of coverage.

Vapor phase reflow and dual wave soldering, utilized with surface mount technology, have imposed solder leach requirements on components that preclude the use of silver-palladium terminations. Best resistance to solder heat is attained using barrier type terminations, which have a nickel layer plated over a silver termination, with a solder or tin protective overcoat to enhance solderability and prevent oxidation of the base metal layer. Capacitors with such terminations will survive molten solder at 260°C with no discernible leaching effect for several minutes versus less than twenty seconds for the best Pd-Ag alloys since nickel is relatively insoluble in Sn, Pb, or Ag and therefore acts as a barrier to solder leaching.

“Thermal expansion mismatch of the chip capacitor and the substrate material results in residual shear stress at the bond.”

#2 Solder Hardness
As described previously, thermal expansion mismatch of the chip capacitor and the substrate material results in residual shear stress at the bond. Theoretical calculations indicate that this stress can exceed 7,000 psi, sufficient to lead to rupture of the chip (if the latter is under tension) or failure of the bond (if the chip is under compression). Fortunately, this condition is alleviated by the ability of the bonding alloy to deform and absorb the majority of the stress. The ductility of the solder alloys is inversely proportional to the hardness of the material; hence, use of softer solders of lower Brinell hardness is desirable.

The most common solder used in hybrid circuit application is Sn62 (62Sn,36Pb,2Ag). Selection of other solders is often predicated on the need for higher temperature tolerance of the circuit, i.e., bonding alloys with higher flow points are mandatory.

Chip Terminations

Capacitor terminations consist of metal-frit (glass) compounds, which are fused to the capacitor body to affect an electrical connection between the internal capacitor electrodes and the circuit pads. Terminations can be classified into the following two general categories:

1. Older thick film silver or silver-palladium (80Ag-20Pd) metallizations
2. The more popular barrier type termination used for surface mount components

The silver-palladium termination has adequate resistance to solder leach and less tendency to tarnish than pure silver terminations. Silver finds application mostly on units destined for axial or radial leading or on specialty items, such as high voltage capacitors that require the use of more ductile silver metal to reduce thermal shock hazards to these units when leaded.

Silver bearing terminations can tarnish. Usually packed with a tarnish retardant paper, capacitors will store indefinitely and solder properly with the appropriate fluxes. Severely tarnished units can be restored to a clean metal finish by refiring of the product to approximately 700°C to 800°C. Note that product supplied in reeled format cannot be effectively protected by tarnish retardant paper, as units stored in bulk; hence, inventory planning or the use of barrier termination is recommended.

Barrier layer terminations are based on plating technology to provide 100 to 150 microinches of nickel thickness over a fired silver termination. As nickel readily oxidizes, a second tin/solder or tin layer 200 to 250 microinches thick is plated over the nickel to protect it and provide a readily solderable surface with good shelf life.

The electrolytic process is perhaps the preferred method of nickel deposition. A current is utilized to deposit nickel from nickel sulfamate and nickel chloride in a boric acid solution onto the silver termination of the capacitor. This termination differs from conventional materials in that the frit that bonds the termination to the capacitor must be chemically resistant to the plating solutions and thus is bismuth free. Such frits do not promote solderability; hence, units with this termination are unsolderable unless properly plated with nickel and solder. Immediately after the nickel process, units must undergo the solder process before the onset of any oxidation of the base metal layer. Units are electroplated using tin and lead concentrates in a deionized water solution.

> **“The distinct advantage of the nickel barrier termination is evident in its name; it serves not only as a guard against solder leach, by virtue of the relatively insoluble nature of nickel in solder alloys, but also forms a barrier to the formation of intermetallic compounds in the solder joint.”**

An electroless method of nickel deposition, based on chemical reduction of nickel boron solutions and catalytic activators, can also provide a continuous nickel barrier layer, but this is not as suitable for tin lead plating. Alternate application of a solder coat by wave soldering methods creates dimensional tolerance difficulties, which is not desirable for components to be taped and reeled for use in surface mount technology

The distinct advantage of the nickel barrier termination is evident in its name; it serves not only as a guard against solder leach, by virtue of the relatively insoluble nature of nickel in solder alloys, but also forms a barrier to the formation of intermetallic compounds in the solder joint, which can adversely affect the long term reliability of the bond. Non-barrier terminations can be affected by a time-dependent diffusion phenomenon of Ag, Pd, and Sn atoms, which accelerate with thermal cycling and can eventually lead to stress cracks separating the component from the assembly.

Capacitors with nickel barrier terminations have been shown to arrest the diffusion process and the formation of intermetallic compounds, hence maintaining the integrity of the bond. Although it is a characteristic of all nickel deposition to retain a contractile or tensile condition, the industry has developed the methods to plate the material with controlled metallographic structure and ductility to produce physical and mechanical properties suitable for all the dielectric types of multilayer capacitors.

Ion Migration

Chip terminations and bonding alloys contain metals (notably silver and tin), that can hydrolyze in the presence of water moisture. Under the influence of an electric field, the hydroxide can dissociate to form metal cations, which have a net positive charge and can migrate to the cathode. This phenomenon occurs with AC voltage as well as with a DC bias, and the severity is directly proportional to the voltage gradient.

Given enough time, a bridge of silver or tin will form between chip terminations, reducing the insulation resistance and eventually forming an electrical short. Avoidance of this problem can be accomplished with the use of very expensive gold terminations and substrate conductors or with the elimination of water moisture from the circuit, which precludes the formation of mobile cations. The latter is accomplished by hermetic sealing of circuits or the use of waterproof encapsulants such as epoxies.

Dissipation Factor and Capacitive Reactance

When it comes to practical applications, a real-world capacitor is not perfect, such that the voltage and current across it will not be perfectly 90 degrees out of phase. The angle by which the current is out of phase from ideal can be determined (Figure 31), and the tangent of this angle is defined as loss tangent or DF.

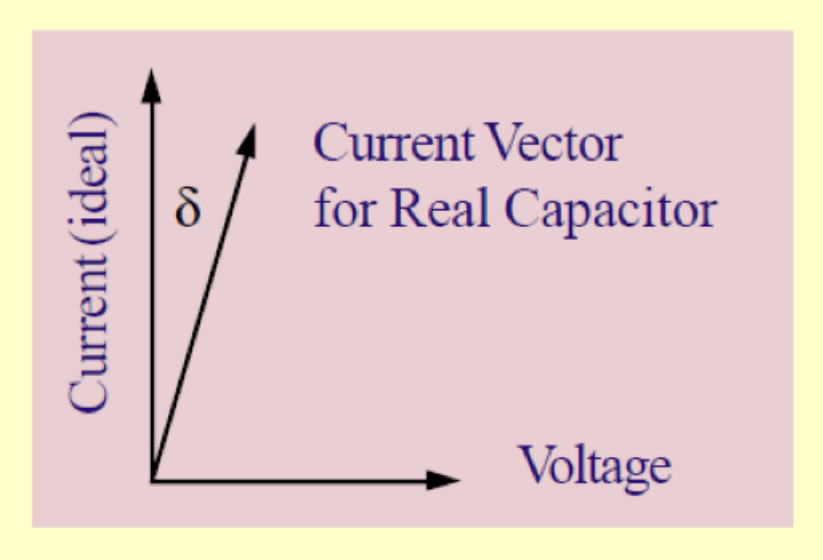

Figure 31. Loss Tangent in a Real-World Capacitor

When it comes to practical applications, a real-world capacitor is not perfect, such that the voltage and current across it will not be perfectly 90 degrees out of phase.

DF is a material property and is not dependent on geometry of a capacitor. DF greatly influences the usefulness of a dielectric in electronic applications. In practice, it is found that lower DF is associated with materials of lower dielectric constant K. Higher K materials, which develop this property by virtue of high polarization mechanisms, display higher DFdissipation factor. Dissipation factorF and quality (Q) are reciprocals of each other and measure the losses with the capacitor.

$$Q = 1/DF$$

where Q is quality factor and DF is dissipation factor.

Because a capacitor is made of two (or more) conductors separated from each other by an insulator, capacitive reactance is a measure of a capacitor's opposition to change in voltage or AC voltage flow.

$$X_c = 1/2\pi fC$$

where is Xc is capacitive reactance in ohms, f is frequency in hertz and C is capacitance in farads.

Equivalent Series Resistance

Equivalent series resistance (ESR) is a measurement of all the nonideal electrical resistances in series with the capacitor, such as the resistance of the conductor plates, insulating material, terminations, and so forth. The higher the ESR, the more losses occur in the capacitor.

$$R_s=DF\times X_c$$

where Rs is ESR in ohms, DF is dissipation factor, and Xc is capacitive reactance in ohms.

ESR also determines how much ripple current is converted into heat generation. High temperatures can adversely affect performance, or unexpectedly damage the capacitor in the long run if power dissipation is not properly handled.

$$P = I^2 R$$

where P is power dissipation in watts, I is root mean square (RMS) current in amps, and R is ESR in ohms.

Selecting the Right Capacitor for Your Specific Application Needs

At the most basic level, capacitors are essentially storage devices for electric energy used in various applications across a variety of industries. However, as shown throughout this eBook, capacitor technology covers a wide range of product types, based on a multitude of dielectric materials and physical configurations, which can be daunting when deciding what capacitor is right for your application.

At Knowles Precision Devices, we manufacture high-performance, high-reliability capacitors using the latest technologies and dielectric materials. As a specialty components manufacturer, we choose to take on complex challenges, which means our experts are ready to help you simplify the process of selecting the right capacitor for your specific application needs. The bottom line is, our capacitors are engineered to reliably meet the specific requirements of your diverse applications, from high-frequency 5G devices to fail-safe medical equipment to high-voltage electric vehicles, and more.

Applications Where You Will Find Knowles Precision Devices Capacitors:

- Microwave Radar
- Medical
- RF
- Test Equipment
- Switch Filter Banks
- Satellite and Radio Communications
- Synthesizer and filter banks
- 5G Base Stations
- HF Frequency Snubber
- Frequency Control/Tuning Impedance Matching
- Modem/Tip and Ring
- Decoupling/Smoothing
- AC Noise Removal
- High-Voltage Circuitry
- High-Speed Decoupling
- Feedthrough Filtering
- Automotive
- Harsh Environments
- Military/Aerospace

If you need help selecting from our portfolio please contact us and we can guide you through the selection process.

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